BS32F030xBx6

DATASHEET

Version: V1.0.3 Date: 17/03/2023

Features

- **48MHz Cortex® -M0+ 32-bit CPU**
- **Memories**
  - 128 Kbytes of Flash memory with read and write protection
  - 8 Kbytes of SRAM
- **Power Supply**
  - VDD = 2.5 to 5.5V
- **Clock & Crystal Oscillator**
  - 32.768kHz external oscillator
  - High-speed Internal 1M RC
  - Low-speed Internal 32K RC
  - 48M PLL
  - SysClock: 48M/24M/12M/6M/3M /1.5M/0.75M
  - IWDG clock source: RC32K
- **Multiple GPIOs**
  - All mappable on external interrupt
- **Timer/Counter**
  - 16-bit advanced control timer(TIM1)
  - Five 16-bit general-purpose timer (TIM3,TIM14,TIM15,TIM16,TIM17)
  - 20-bit basic timer (TIM6)
  - Independent watchdog (IWDG)
  - Window watchdog (WWDG)
  - SysTick timer
- **RTC with alarm and calender**
- **Communication interfaces**
  - Two UART standard interfaces, independent clock.
  - Two SPI standard interfaces with master/slave
  - Two I2C standard interfaces with master/slave, supporting fast mode of 1Mb/s
- **32-channel DMA controller with mapping**
- **12-bit, 1.0μs ADC (multiple channels)**
- **CRC calculation unit**
- **Reset**
  - Power-on/Power-down reset (POR/PDR)
  - Brown-out Reset (BOR)
  - Soft Reset
  - Watchdog Reset
  - External Pin Reset
  - Shutdown Reset
- **Operating Modes**
  - Active mode
  - Low-power modes:
    - ❖Sleep
    - ❖Sleepdeep
    - ❖Shutdown
- **Serial Wire Debug (SWD)**
- **Operating Conditions**
  - 2.5 to 5.5V
  - - 40℃ to 85℃
- **Packages**: LQFP48/LQFP32/QFN32

Part Number

BS32F030CBT6	BS32F030KBT6
BS32F030KBU6	

Table of contents

List of tables

List of figures

1 Introduction

This document provides information on BS32F030xBx6 microcontroller, such as parameters, functional modules, electrical characteristics and ordering information.

BS32F030 series microcontroller are based on ARM® Cortex®-M0+ 32-bit core operating at up to 48 MHz frequency, embedded with 128K bytes of Flash memory and 8K bytes of SRAM. BS32F030xBx6 series are available in three packages with 32 and 48 pins, such as LQFP48, LQFP32 and QFN32. The devices offer six 16-bit timers (one advanced-control timer, five general-purpose timers), a 20-bit timer. The devices offer multiple standard communication interfaces (two UART, two I^2Cs, and two SPI).

BS32F030 series operate within ambient temperatures from -40 to 85℃ and with supply voltages from 2.5 V to 5.5V. The devices offers different operating modes to meet the power consumption requirement in various cases.

BS32F030 series microcontrollers are suitable for many applications such as medical and handheld devices, PC gaming peripherals, GPS, alert system, video and audio system, and heating ventilation air conditioning, printer and scanners.

2 Features

Table 2.1 BS32F030xBx6 functions and configurations

Peripherals		BS32F030xBx6		
Flash (KB)		128		
SRAM (KB)		8		
Maximum CPU Frequency		48MHz		
GPIO		39	25	27
EXTI		0 to 15		
Timer	Advanced-control timer (1)	1 (16-bit)		
	General-purpose Timer (2)	5 (16-bit)		
	Basic Timer(3)	1 (20-bit)		
Communication Interfaces	SPI	2		
	I2C	2		
	UART	2		
12-bit ADC (channel number)		One 41-channel (39 external input channels + 1 internal reference voltage channel + 1 internal temperature sensor channel) ADC	One 27-channel (25 external input channels + 1 internal reference voltage channel + 1 internal temperature sensor channel) ADC	One 29-channel (27 external input channel + 1 internal eference voltage channe + 1 internal temperature sensor channel)ADC
DMA		Single AHB master, 32 independent channels configurable		
RTC		Programmable Alarm A, 2 external tamper check		
CRC		Three CRCs with polynomial options		
Conditions	Operating Temperature	Ambient Temperature:-40℃ to +85°C Conjunction Temperature: -40℃ to +105°C		
	Operating Voltage	2.5V to 5.5V		
Package Information		LQFP48	LQFP32	QFN32

1. TIM1
2. TIM3/TIM14/TIM15/TIM16/TIM17
3. TIM6

3 Pinouts and Pin Description

3.1 BS32F030xBx6 Pin package and function definition

Figure 3.1 BS32F030CBT6 package pins

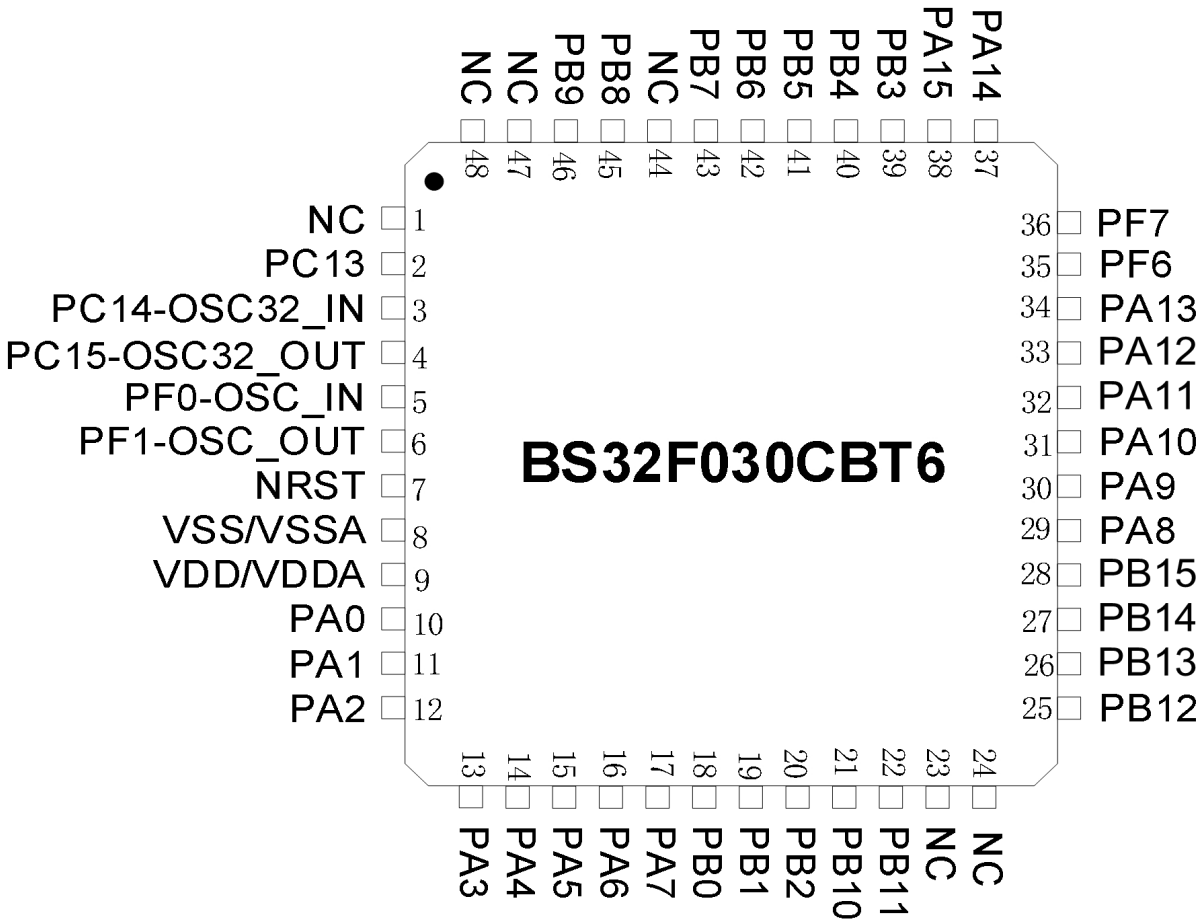


Figure 3.2 BS32F030KBT6 package pins

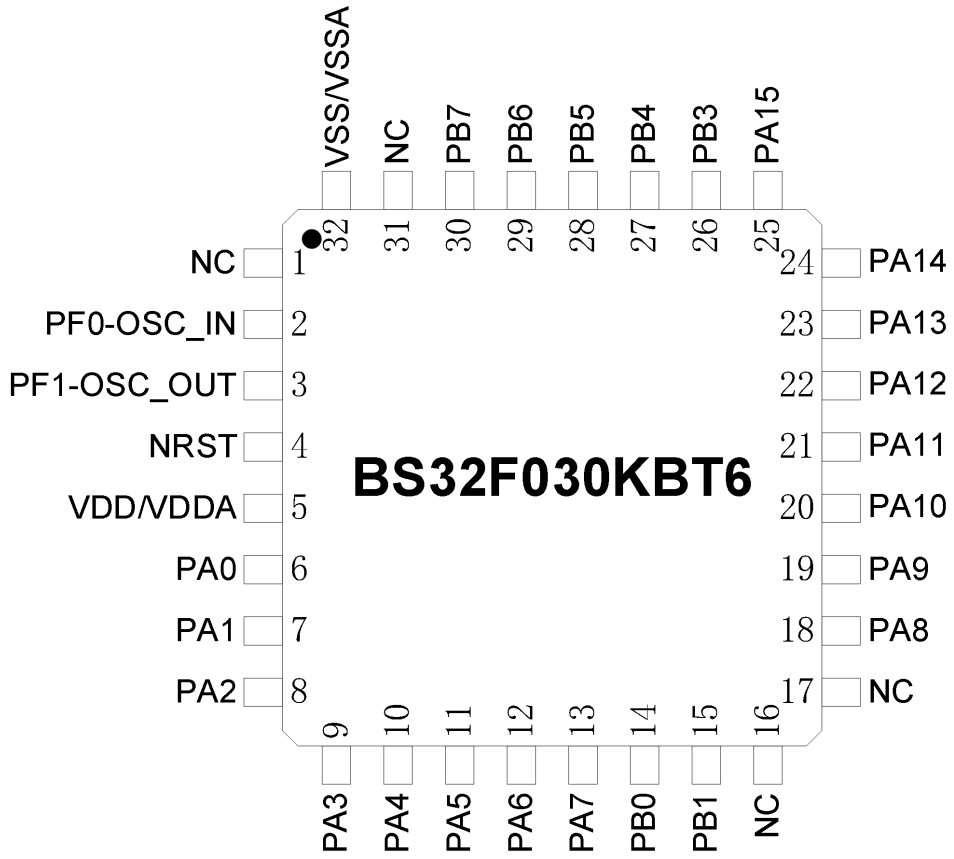


Figure 3.3 BS32F030KBU6 package pins

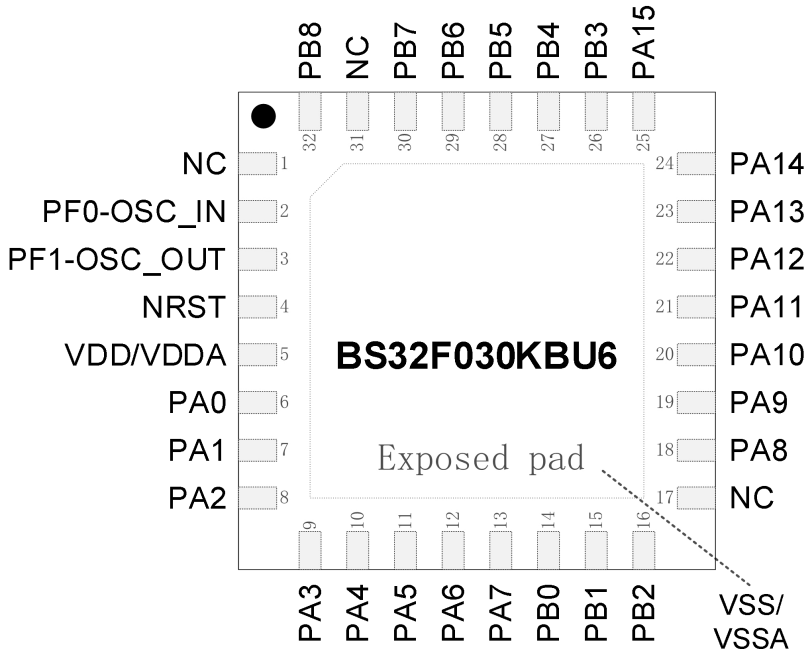


Table 3.1 BS32F030xBx6 pin definitions

Pin number			Pin name	Pin type	Note	Pin functions		
LQFP48	LQFP32	QFN32				Default functions	Alternate functions	Additional functions
1	1	1	-	-	-	-	-	-
2	-	-	PC13	I/O	-	PC13	TIM1_BKIN	ADC_IN34/RTC_OUT/ TAMP_IN1/WKUP2
3	-	-	PC14	I/O	-	PC14	TIM1_BKIN2	ADC_IN35/OSC32_IN/ OSC_IN (1)
4	-	-	PC15	I/O	-	PC15	OSC32_EN/OSC_EN/ TIM15_BKIN	ADC_IN36 /OSC32_OUT
5	2	2	PF0	I/O	-	PF0	TIM14_CH1	ADC_IN41/OSC_IN
6	3	3	PF1	I/O	-	PF1	OSC_EN/TIM15_CH1N	ADC_IN42/OSC_OUT
7	4	4	NRST	I	-	NRST	-	-
8	32	-	VSS/VSSA	S	-	VSS/VSSA	-	-
9	5	5	VDD/VDDA	S	-	VDD/VDDA	-	-
10	6	6	PA0	I/O	-	PA0	SPI2_SCK/UART2_CTS	ADC_IN0/TAMP_IN2/ WKUP1
11	7	7	PA1	I/O	-	PA1	SPI1_SCK/UART2_RTS_DE/ TIM15_CH1N	ADC_IN1
12	8	8	PA2	I/O	-	PA2	SPI1_MOSI/UART2_TX/ TIM15_CH1	ADC_IN2/WKUP4
13	9	9	PA3	I/O	-	PA3	SPI2_MISO/UART2_RX/ TIM15_CH2	ADC_IN3
14	10	10	PA4	I/O	-	PA4	SPI1_NSS/SPI2_MOSI/ TIM14_CH1	ADC_IN4/RTC_OUT2 TAMP_IN1
15	11	11	PA5	I/O	-	PA5	SPI1_SCK	ADC_IN5
16	12	12	PA6	I/O	-	PA6	SPI1_MISO/TIM3_CH1/ TIM1_BKIN/TIM16_CH1	ADC_IN6
17	13	13	PA7	I/O	-	PA7	SPI1_MOSI/TIM3_CH2/ TIM1_CH1N/TIM14_CH1/ TIM17_CH1	ADC_IN7

Table 3.1 BS32F030xBx6 pin definitions (continued)

Pin number			Pin name	Pin type	Note	Pin functions		
LQFP48	LQFP32	QFN32				Default functions	Alternate functions	Additional functions
18	14	14	PB0	I/O	-	PB0	SPI1_NSS/TIM3_CH3/ TIM1_CH2N	ADC_IN16
19	15	15	PB1	I/O	-	PB1	TIM14_CH1/TIM3_CH4/ TIM1_CH3N	ADC_IN17
20	-	16	PB2	I/O	-	PB2	SPI2_MISO	ADC_IN18
21	-	-	PB10	I/O	-	PB10	SPI2_SCK /I2C2_SCL	ADC_IN26
22	-	-	PB11	I/O	-	PB11	SPI2_MOSI/I2C2_SDA	ADC_IN27
23	16	-	-	-	-	-	-	-
24	17	17	-	-	-	-	-	-
25	-	-	PB12	I/O	-	PB12	SPI2_NSS/TIM1_BKIN/ TIM15_BKIN	ADC_IN28
26	-	-	PB13	I/O	-	PB13	SPI2_SCK/TIM1_CH1N/ TIM15_CH1N/I2C2_SCL	ADC_IN29
27	-	-	PB14	I/O	-	PB14	SPI2_MISO/TIM1_CH2N/ TIM15_CH1/I2C2_SDA	ADC_IN30
28	-	-	PB15	I/O	-	PB15	SPI2_MOSI/TIM1_CH3N/ TIM15_CH1N/TIM15_CH2	ADC_IN31
29	18	18	PA8	I/O	-	PA8	MCO/SPI2_NSS/TIM1_CH1	ADC_IN8
30	19	19	PA9	I/O	-	PA9	MCO/UART1_TX/TIM1_CH2/ SPI2_MISO/TIM15_BKIN/ I2C1_SCL	ADC_IN9
31	20	20	PA10	I/O	-	PA10	SPI2_MOSI/UART1_RX/ TIM1_CH3/TIM17_BKIN/ I2C1_SDA	ADC_IN10
32	21	21	PA11	I/O	-	PA11	SPI1_MISO/UART1_CTS/ TIM1_CH4/TIM1_BKIN2/ I2C2_SCL	ADC_IN11
33	22	22	PA12	I/O	-	PA12	SPI1_MOSI/UART1_RTS_DE TIM1_ETR/I2C2_SDA	ADC_IN12
34	23	23	PA13	I/O	-	SWDIO	-	ADC_IN13
35	-	-	PF6	I/O	-	PF6	I2C2_SCL	ADC_IN43

Table 3.1 BS32F030xBx6 pin definitions (continued)

Pin number			Pin name	Pin type	Note	Pin functions		
LQFP48	LQFP32	QFN32				Default functions	Alternate functions	Additional functions
36	-	-	PF7	I/O	-	PF7	I2C2_SDA	ADC_IN44
37	24	24	PA14	I/O	-	SWCLK	UART2_TX	ADC_IN14
38	25	25	PA15	I/O	-	PA15	SPI1_NSS/UART2_RX	ADC_IN15
39	26	26	PB3	I/O	-	PB3	SPI1_SCK/TIM1_CH2/ UART1_RTS_DE	ADC_IN19
40	27	27	PB4	I/O	-	PB4	SPI1_MISO/TIM3_CH1/ UART1_CTS/TIM17_BKIN	ADC_IN20
41	28	28	PB5	I/O	-	PB5	SPI1_MOSI/TIM3_CH2/ TIM16_BKIN	ADC_IN21/WKUP6
42	29	29	PB6	I/O	-	PB6	UART1_TX/TIM1_CH3/ TIM16_CH1N/SPI2_MISO/ I2C1_SCL	ADC_IN22
43	30	30	PB7	I/O	-	PB7	UART1_RX/SPI2_MOSI/ TIM17_CH1N/I2C1_SDA	ADC_IN23
44	31	31	-	-	-	-	-	-
45	-	32	PB8	I/O	-	PB8	SPI2_SCK/TIM16_CH1/ TIM15_BKIN/I2C1_SCL	ADC_IN24
46	-	-	PB9	I/O	-	PB9	TIM17_CH1/SPI2_NSS/ I2C1_SDA	ADC_IN25
47	-	-	-	-	-	-	-	-
48	-	-	-	-	-	-	-	-

1. PC14 multiplexes input from OSC_HSE,Valid when HSEON and HSEBYPS set to 1.

Table 3.2 Port A alternate and additional functions

GPIO	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	Configurations (Priority from high to low)		
PA0	SPI2_SCK	UART2_CTS	-	-	-	-	-	-	ADC_IN0	TAMP_IN2	WKUP1
PA1	SPI1_SCK	UART2_RTS_DE	-	-	-	TIM15_CH1N	-	-	ADC_IN1	-	-
PA2	SPI1_MOSI	UART2_TX	-	-	-	TIM15_CH1	-	-	ADC_IN2	WKUP4	-
PA3	SPI2_MISO	UART2_RX	-	-	-	TIM15_CH2	-	-	ADC_IN3	-	-
PA4	SPI1_NSS	SPI2_MOSI	-	-	TIM14_CH1	-	-	-	ADC_IN4	RTC_OUT	TAMP_IN1
PA5	SPI1_SCK	-	-	-	-	-	-	-	ADC_IN5	-	-
PA6	SPI1_MISO	TIM3_CH1	TIM1_BKIN	-	-	TIM16_CH1	-	-	ADC_IN6	-	-
PA7	SPI1_MOSI	TIM3_CH2	TIM1_CH1N	-	TIM14_CH1	TIM17_CH1	-	-	ADC_IN7	-	-
PA8	MCO	SPI2_NSS	TIM1_CH1	-	-	-	-	-	ADC_IN8		-
PA9	MCO	UART1_TX	TIM1_CH2	-	SPI2_MISO	TIM15_BKIN	I2C1_SCL	-	ADC_IN9		-
PA10	SPI2_MOSI	UART1_RX	TIM1_CH3	-	-	TIM17_BKIN	I2C1_SDA	-	ADC_IN10	-	-
PA11	SPI1_MISO	UART1_CTS	TIM1_CH4	-	-	TIM1_BKIN2	I2C2_SCL	-	ADC_IN11	-	-
PA12	SPI1_MOSI	UART1_RTS_DE	TIM1_ETR	-	-	-	I2C2_SDA	-	ADC_IN12	-	-
PA13	SWDIO	-	-	-	-	-	-	-	ADC_IN13	-	-
PA14	SWCLK	UART2_TX	-	-	-	-	-	-	ADC_IN14	-	-
PA15	SPI1_NSS	UART2_RX	-	-	-	-	-	-	ADC_IN15	-	-

Table 3.3 Port B alternate and additional functions

GPIO	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	Configurations (Priority from high to low)		
PB0	SPI1_NSS	TIM3_CH3	TIM1_CH2N	-	-	-	-	-	ADC_IN16	-	-
PB1	TIM14_CH1	TIM3_CH4	TIM1_CH3N	-	-	-	-	-	ADC_IN17	-	-
PB2	-	SPI2_MISO	-	-	-	-	-	-	ADC_IN18	-	-
PB3	SPI1_SCK	TIM1_CH2	-	-	UART1_RTS_DE	-		-	ADC_IN19	-	-
PB4	SPI1_MISO	TIM3_CH1	-	-	UART1_CTS	TIM17_BKIN	-	-	ADC_IN20	-	-
PB5	SPI1_MOSI	TIM3_CH2	TIM16_BKIN	-	-	-	-	-	ADC_IN21	WKUP6	-
PB6	UART1_TX	TIM1_CH3	TIM16_CH1N	-	SPI2_MISO	-	I2C1_SCL	-	ADC_IN22	-	-
PB7	UART1_RX	SPI2_MOSI	TIM17_CH1N	-	-	-	I2C1_SDA	-	ADC_IN23	-	-
PB8	-	SPI2_SCK	TIM16_CH1	-	-	TIM15_BKIN	I2C1_SCL	-	ADC_IN24	-	-
PB9	-	-	TIM17_CH1	-	-	SPI2_NSS	I2C1_SDA	-	ADC_IN25	-	-
PB10	-	-		-	-	SPI2_SCK	I2C2_SCL	-	ADC_IN26	-	-
PB11	SPI2_MOSI	-		-	-		I2C2_SDA	-	ADC_IN27	-	-
PB12	SPI2_NSS	-	TIM1_BKIN	-	-	TIM15_BKIN		-	ADC_IN28	-	-
PB13	SPI2_SCK	-	TIM1_CH1N	-	-	TIM15_CH1N	I2C2_SCL	-	ADC_IN29	-	-
PB14	SPI2_MISO	-	TIM1_CH2N	-	-	TIM15_CH1	I2C2_SDA	-	ADC_IN30	-	-
PB15	SPI2_MOSI	-	TIM1_CH3N	-	TIM15_CH1N	TIM15_CH2	-	-	ADC_IN31	-	-

Table 3.4 Port C alternate and additional functions

GPIO	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	Configurations (Priority from high to low)			
PC13	-	-	TIM1_BKIN	-	-	-	-	-	ADC_IN34	RTC_OUT	TAMP_IN1	WKUP2
PC14	-	-	TIM1_BKIN2	-	-	-	-	-	ADC_IN35	OSC32_IN	OSC_IN	-
PC15	OSC32_EN	OSC_EN	TIM15_BKIN	-	-	-	-	-	ADC_IN36	OSC32_OUT	-	-

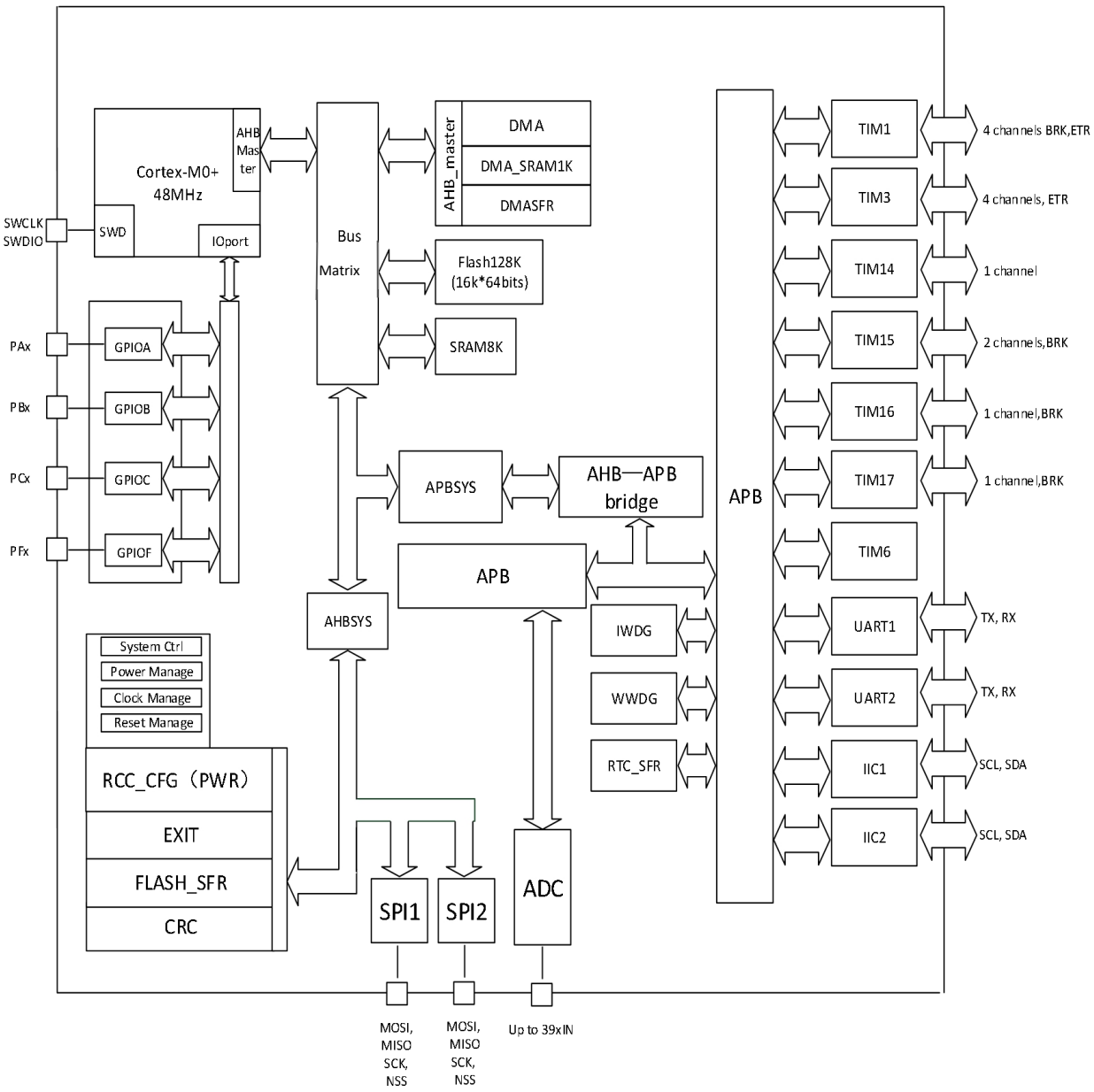
Table 3.5 Port F alternate and additional functions

GPIO	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	Configurations (Priority from high to low)			
PF0	-	-	TIM14_CH1	-	-	-	-	-	ADC_IN41	OSC_IN	-	-
PF1	OSC_EN	-	TIM15_CH1N	-	-	-	-	-	ADC_IN42	OSC_OUT	-	-
PF6	I2C2_SCL	-	-	-	-	-	-	-	ADC_IN43	-	-	-
PF7	I2C2_SDA	-	-	-	-	-	-	-	ADC_IN44	-	-	-

4 Block Diagram

BS32F030xBx6 series microcontrollers are equipped with many peripherals, which have AHB and APB buses. Different peripherals are on the different buses according to functional requirements to improve the efficiency of the system running. Figure 4.1 shows the system block diagram.

Figure 4.1 BS32F030xBx6 block diagram



5 Memory Map

System allocates different address space to different peripherals, refer to Reference Manual. Table 5.1 shows a table of address mapping.

Table 5.1 List of address mapping

Type	Module	Base address	End address	Size
IOPORT	GPIOF	0x5000_1400	0x5000_17FF	1KB
	reserve	0x5000_1000	0x5000_13FF	1KB
	GPIOD	0x5000_0C00	0x5000_0FFF	1KB
	GPIOC	0x5000_0800	0x5000_0BFF	1KB
	GPIOB	0x5000_0400	0x5000_07FF	1KB
	GPIOA	0x5000_0000	0x5000_03FF	1KB
APB	TIM17	0x4001_4800	0x4001_4BFF	1KB
	TIM16	0x4001_4400	0x4001_47FF	1KB
	TIM15	0x4001_4000	0x4001_43FF	1KB
	UART1	0x4001_3800	0x4001_3BFF	1KB
	TIM1	0x4001_2C00	0x4001_2FFF	1KB
	ADC	0x4001_2400	0x4001_27FF	1KB
	I2C2	0x4000_5800	0x4000_5BFF	1KB
	I2C1	0x4000_5400	0x4000_57FF	1KB
	UART2	0x4000_4400	0x4000_47FF	1KB
	IWDG	0x4000_3000	0x4000_33FF	1KB
	WWDG	0x4000_2C00	0x4000_2FFF	1KB
	RTC	0x4000_2800	0x4000_2BFF	1KB
	TIM14	0x4000_2000	0x4000_23FF	1KB
	TIM6	0x4000_1000	0x4000_13FF	1KB
	TIM3	0x4000_0400	0x4000_07FF	1KB
AHB	DMA_SFR	0x4003_0400	0x4003_07FF	1KB
	DMA_SRAM	0x4003_0000	0x4003_03FF	1KB
	SPI2	0x4002_A400	0x4002_A7FF	1KB
	SPI1	0x4002_A000	0x4002_A3FF	1KB
	CRC	0x4002_3000	0x4002_33FF	1KB
	FLASH	0x4002_2000	0x4002_23FF	1KB
	EXTI	0x4002_1800	0x4002_1BFF	1KB
	RCC	0x4002_1000	0x4002_13FF	1KB
AHB2APB	AHB2APB	0x4000_0000	0x4001_63FF	89KB
SRAM	SRAM	0x2000_0000	0x2000_1FFF	8KB
CODE	System information block	0x0002_0200	0x0002_03FF	512B
	Option byte block	0x0002_0000	0x0002_01FF	512B
	FLASH	0x0000_0000	0x0001_FFFF	128KB

6 Functional Overview

6.1 ARM® Cortex® -M0+ Core

The Cortex-M0+ is an ARM Cortex processor with a Von Neumann architecture, including a lean instruction set to improve efficiency. It provides a higher code density and extensively optimized design than other 8-bit and 16-bit microcontrollers, and is compatible with other Cortex-M products.

ARM® Cortex® -M0+ Core is widely used in design of embedded products, with integrated Memory Protection Unit (MPU) and ultra-low power consumption, supporting KEIL&IAR mainstream development tools, which is easy for developers to program, implement and debug the product functions.

6.2 Flash memory

BS32F030xBx6 devices offer a 128Kbytes of Flash memory for storing code and data, without ECC function.

Flash memory supports IAP Boot upgrade.

Flexible protections can be configured thanks to option bytes:

- Readout protection (RDP) to protect the whole memory. Two levels are available:
  - Level 0: no readout protection
  - Level 1: enable readout protection
- Write protection (WRP): The minimum protection area is pages, and the page size is 512 bytes. Protect the page from being erased and programmed.

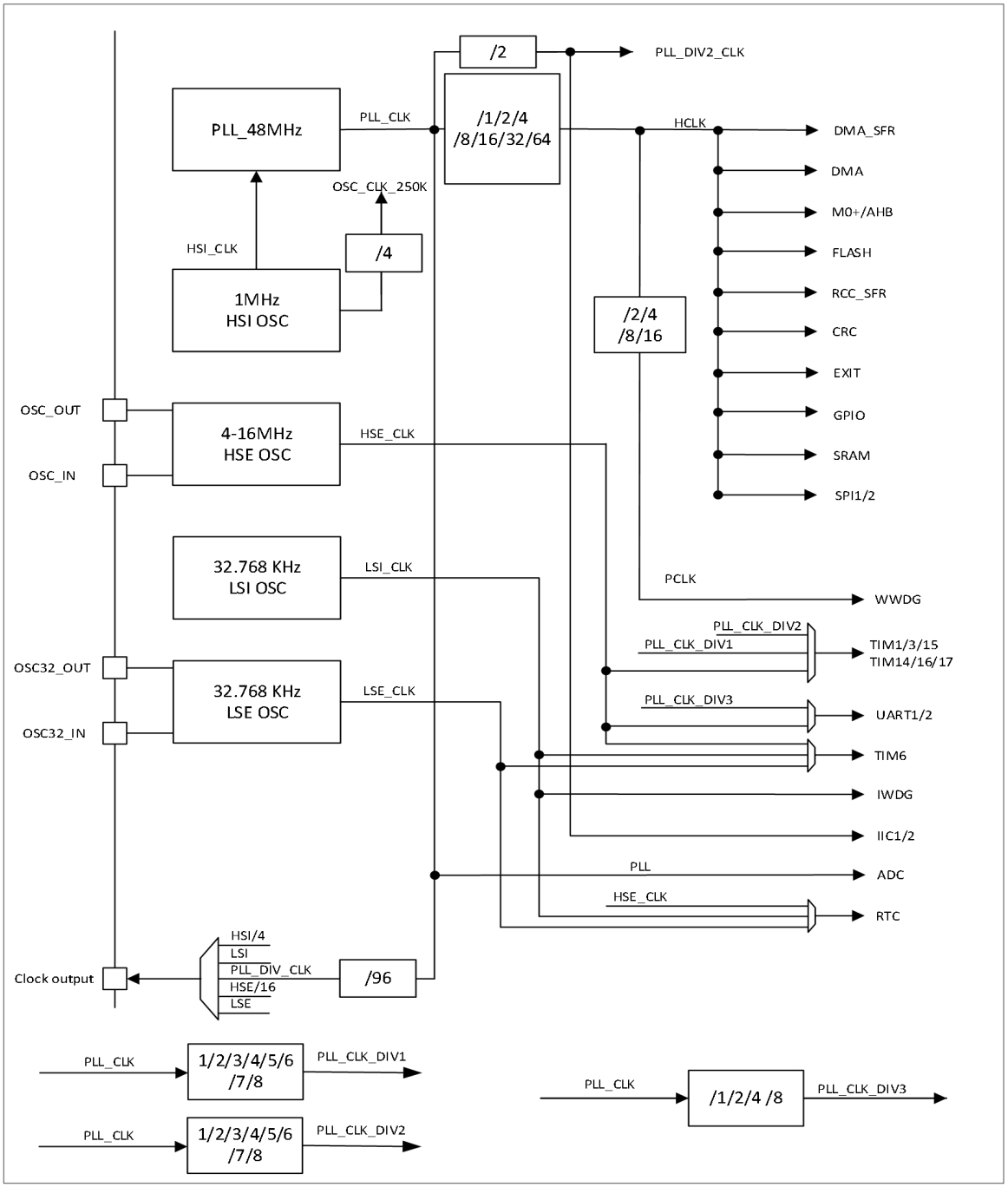
6.3 SRAM

BS32F030xBx6 devices offer 8Kbytes of SRAM. The address ranges form 0x2000_0000 to 0x2000_1FFF.

6.4 Clock

System clock source is 1MHz internal RC oscillator, which is multiplexed to generate PLL, supplying clock to the Core and the peripherals. It also manages low-power mode by clock gating and multi-level prescalers , to ensures clock robustness. The clock source of IWDG is always LSI.

Figure 6.1 BS32F030xBx6 system clock tree



6.5 Power management

6.5.1 Power supply

BS32F030xBx6 devices require a operating voltage (V_{DD}) of 2.5V to 5.5V, power supply scheme:

- V_{DD}=2.5V to 5.5V

6.5.2 Power supply monitor

The device has an integrated power-on/power-down (POR/PDR) reset , the power-down threshold of BOR is configurable, active in all power.

The integrated LVDT threshold is also configurable.

6.5.3 Low-power Modes

By default, the microcontrollers is in Run mode after system or power reset. It is up to the user to select one of the low-power modes as follows:

- Sleep Mode
- Deepsleep Mode
- Shutdown Mode

Table 6.1 Low-power mode and wake-up sources

Low-power mode and wake-up sources	**Sleep Mode:** - All operating peripherals interrupt - IWDG reset - BOR reset - NRST external reset
	Deepsleep: - Any interrupts on EXTI line - TIM6 interrupt - RTC/TAMP interrupt - I2C interrupt - UART interrupt - LVDT interrupt - IWDG reset - BOR reset - NRST external reset
	Shutdown: - WKUP pin - RTC/TAMP interrupt - NRST external reset - BOR reset

6.6 Direct memory access controller (DMA)

The direct memory access (DMA) controller is a bus master and system peripheral with Single-AHB architecture.

It contains a Single-AHB master and 32 channels independently configurable.

- Each DMA channel with two-level priority configurable
- Support DMA data transfers as follows:
  - Memory-to-memory
  - Memory-to-peripheral
  - Peripheral-to-memory
- Support three DMA data transfer size: word, half-word, byte.
- The number of data to be transferred in a single DMA cycle is from 1 to 1024, the unit depends on the data transfer size.
- An interrupt is generated when any channel that completes the data transfer or occurs bus error, each channel has an independent interrupt enable, transfer finish flag and error flag.

6.7 Cyclic redundancy check calculation unit (CRC)

CRC (cyclic redundancy check) calculation unit is used to get a CRC code using a configurable generator polynomial value and size.

Among other applications, CRC based techniques are used to verify data transmission or storage integrity. In the scope of the EN/IEC 60335-1 standard, they offer a means of verifying the Flash memory integrity. The CRC calculation unit helps compute a signature of the software in real-time, to be compared with a reference signature generated at link Time.

- Three CRC polynomial options:
  - CRC-32: polynomial 32'h04C11DB7 (by default)
  - CRC-16: polynomial 16'h1021
  - CRC-8: polynomial 8'h07
- Handles 8-, 16-, 32-bit data size:
  - 4 AHB clock cycles for 32-bit
  - 2 AHB clock cycles for 16-bit
  - 1 AHB clock cycles for 8-bit

- Initial value, XOR value configurable

6.8 General-purpose inputs/outputs (GPIO)

Each GPIO pin of BS32F030xBx6 can be configured as output/input or as peripheral alternate function (AF). All GPIO pins can be mapped to external interrupts. Most of the GPIO pins have special digital or analog functions.

- Output states: push-pull or open drain output,with pull-up/pull-down resistors
- Input states: Float input with pull-up/pull-down resistor, analog input
- Each of the GPIO pins with speed options (2M/10M/50M)
- 40K pull-up/down resistor

6.9 Interrupts

The device flexibly manages events causing interrupts of linear program execution, called interrupts. The Cortex-M0+ processor core, a nested vectored interrupt controller (NVIC) and an extended interrupt/event controller (EXTI) are used to handle the interrupts. Interrupts result in interrupting the program flow, executing an interrupt service routine (ISR) then resuming the original program flow.

6.9.1 Nested vectored interrupt controller (NVIC)

The configurable nested vectored interrupt controller is tightly coupled with the M0+ core. It handles physical line events associated with a non-maskable interrupt (NMI) and maskable interrupts, and Cortex-M0+ interrupts. It provides flexible priority management.

The tight coupling of the processor core with NVIC significantly reduces the latency between interrupt events and enter an interrupt service function (ISR). The ISR vectors are listed in a vector table, stored in the NVIC at a base address. The vector address of an ISR to execute is hardware-built from the vector table base address and the ISR order number used as offset.

If a lower-priority interrupt event occurs and is ready to execute before a higher priority interrupt event occurs, the later higher priority interrupt event executes first. There is also an optimization called tail biting. Upon a return from a higher-priority ISR then start of a pending lower-priority ISR, the unnecessary processor context stack and pending is skipped. This reduces latency and contributes to power efficiency.

Features of the NVIC:

- Low-latency interrupt processing
- 4 priority levels

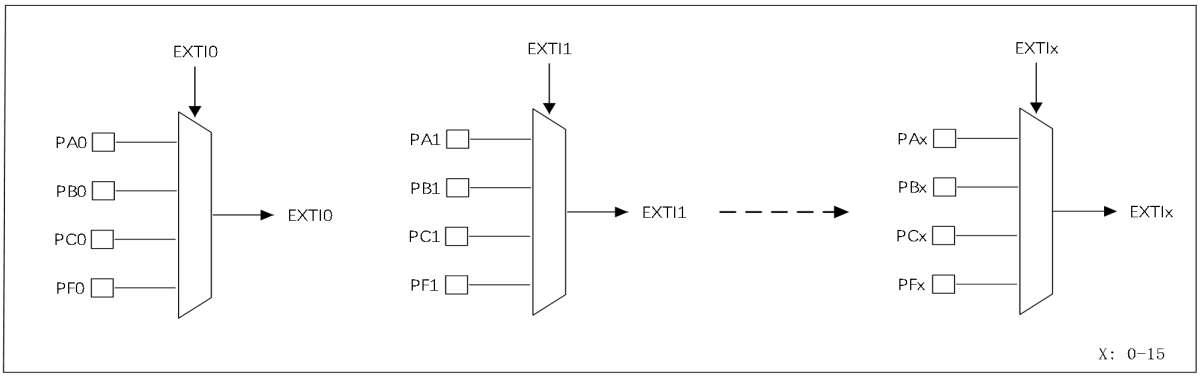
- Handling of a Non-maskable interrupt
- Handling of 32 maskable interrupt lines
- Handling of 10 Cortex-M0+ exceptions
- Later-arriving higher-priority interrupt processed first
- tail biting
- Interrupt vector retrieval by hardware

6.9.2 External interrupt controller (EXIT)

The extended interrupt controller adds flexibility in handling physical line events and allows processor wakeup from Low-power mode.

- System wakeup upon event on any input
- Selectable interrupt trigger edge (rising, falling, both edges)
- Detection of trigger edge wakeup system
- Independent rising and falling edge interrupt pending status bits
- Individual interrupt generation mask, used for conditioning the CPU wakeup
- Interrupts (EXIT Lines 0-15) with GPIO interrupt source selectable

Figure 6.2 EXTI GPIO multiplexer



1. Part of pins from 0 to 15 are not shown here, refer to Figure 6.2 for existing configurations.
2. The output of EXTI multiplexer can be used as the output signal of EXTI.

6.10 Analog-to-digital converter (ADC)

BS32F030xBx6 devices embedded a successive approximation ADC with 8-bit (its data resolution is right-aligned) and12-bit selectable. For package LQFP48, the ADC has up to 41 channels (39 external inputs, 1 internal reference voltage and 1 internal temperature sensor). For LQFP32, the ADC has up to 27 channels (25 external inputs + 1 from internal reference voltage + 1 internal temperature sensor). For QFN32, it has up to 29 channels

(27 external inputs + 1 internal reference voltage + 1 internal temperature sensor).

ADC can be performed in single mode and continuous multi-channel DMA mode with the sampling time and conversion rate configurable.

ADC generates an interrupt upon the conversion finishes. The event trigger indicates that the start of the conversion is triggered by software or hardware.

ADC supports wakeup from Sleep Mode.

Way to start the conversion:

- Triggered by software
- Triggered by hardware (internal event:Timer1 event)

6.11 Timers and watchdogs

The BS32F030xBx6 includes an advanced-control timer (TIM1), five general-purpose timers (TIM3, TIM14, TIM15, TIM16, TIM17), a basic timer, two watchdog timers and a SysTick timer. For details, see table 6.2 timer comparson.

Table 6.2 BS32F030xBx6 Timer Comparison

Timer Type	Timer	Counter Resolution	Counter Type	Prescaler Factor	DMA Request Generation	Capture /compare channels	Dead time complementary output channels
Advanced-control	TIM1	16-bit	Up, Down, Up/down	Any integer from 1 to 65536	Yes	4	3
General-purpose	TIM3	16-bit	Up, Down, Up/down	Any integer from 1 to 65536	Yes	4	0
General-purpose	TIM14	16-bit	Up	Any integer from 1 to 65536	-	1	0
General-purpose	TIM15	16-bit	Up	Any integer from 1 to 65536	Yes	2	1
General-purpose	TIM16 TIM17	16-bit	Up	Any integer from 1 to 65536	Yes	1	1
Basic	TIM6	20-bit	Up	-	-	-	

6.11.1 Advanced-control timer (TIM1)

The advanced-control timer features include 16-bit up, down, up/down auto-reload counter, 16-bit programmable prescaler allowing dividing the counter clock frequency by any integer between 1 to 65536.

Up to 6 independent channels for:

- Input capture (but channel 5 and 6)
- Output compare
- PWM generation (edge- and center-aligned modes)
- one-pulse mode output

The advanced-control timer (TIM1) offers Complementary outputs with programmable dead-time complementary output and 2 break inputs to put the timer's output signals in a safe user selectable configuration.

TIM1 control the timer with external signals and synchronization circuit for interconnection of multiple timers. It also has a repetition counter that updates the timer registers only after a given number of counting cycles.

Interrupt/DMA request generation upon the following events:

- Update event: counter overflow, counter initialization (by software or internal/external trigger)
- Trigger event: (counter start, stop, initialization or count by internal/external trigger)
- Input capture
- Output compare

The advanced-control timer can be used to triggering ADC, and supports incremental (quadrature) encoder and Hall-sensor circuitry for positioning purposes.

Trigger input can serve as an external clock or cycle-by-cycle current management.

6.11.2 General-purpose timer (TIM3)

TIM3 timer features include:

➢ 16-bit up, down, up/down auto-reload counter, 16-bit programmable prescaler, the division coefficient of the counter clock frequency is any integer between 1 to 65536.

➢ Up to 4 independent channels for:

- Input capture
- Output compare
- PWM generation (edge- and center-aligned modes)
- one-pulse mode output

- The synchronization circuit of interconnection multiple timers can be realized by using external signal to control the timer.
- Interrupt/DMA generation on the following events:
  - Update: counter overflow, counter initialization (by software or internal/external trigger)
  - Trigger event: (counter start, stop, initialization or count by internal/external trigger)
  - Input capture
  - Output compare
- Supports incremental (quadrature) encoder and hall-sensor circuitry for positioning Purposes.
- Trigger input for external clock or cycle-by-cycle current management

6.11.3 General-purpose timer (TIM14)

TIM14 features include:

- 16-bit up auto-reload counter, 16-bit programmable prescaler. the division coefficient of the counter clock frequency is any integer between 1 to 65536. Only one independent channels for:
  - Input capture
  - Output compare
  - PWM generation (edge-aligned mode)
  - one-pulse mode output
- Interrupt generation on the following events:
  - Update: counter overflow, counter initialization (by software trigger)
  - Input capture
  - Output capture

6.11.4 General-purpose timer (TIM15)

TIM15 timer features include:

- 16-bit up auto-reload counter
- 16-bit programmable prescaler. the division coefficient of the counter clock frequency is any integer between 1 to 65536.
- 2 independent channels for:
  - Input capture
  - Output compare

- PWM generation (edge-aligned mode)
- one-pulse mode output

- Complementary outputs with programmable dead-time (only for channel 1)
- The synchronization circuit of interconnection multiple timers can be realized by using external signal to control the timer.
- repetition counter to update the timer registers only after a given number of cycles of the counter.
- one break input to put the timer's output signals in a safe user selectable configuration.
- Interrupt/DMA request generation upon the following events:
  - Update: counter overflow, counter initialization (by software or internal/external trigger)
  - Trigger event: (counter start, stop, initialization or count by internal/external trigger)
  - Input capture
  - Output compare
  - Break input (interrupt request only)

6.11.5 General-purpose timer (TIM16,17)

The TIM16/TIM17 times include the following features:

- 16-bit up, down, up/down auto-reload counter
- 16-bit programmable prescaler. the division coefficient of the counter clock frequency is any integer between 1 to 65536.
- One independent channel for:
  - Input capture
  - Output compare
  - PWM generation (edge-aligned mode)
  - One-pulse mode output
- Complementary outputs with programmable dead-time
- A break input to put the timer's output signals in a safe user selectable configuration.
- repetition counter to update the timer registers only after a given number of cycles of the counter
- Interrupt/DMA request generation upon the following events:
  - Update: counter overflow, counter initialization (by software trigger)
  - Input capture
  - Output compare
  - Break input (interrupt request only,no DMA request)

6.11.6 Basic timer (TIM6)

The basic timer (TIM6) consists of a 20-bit up auto-reload counter, the clock source includes LSI, LSE or HSE. Refer to Figure 6.1 BS32F030xBx6 System clock tree for details.

System can be timing woken up in Deepsleep Mode.

6.11.7 Independent watchdog (IWDG)

The independent watchdog has a 12-bit up counter with a prescaler factor configurable options (4/8/16/32/64/128/256). The maximum counting value is configurable. The maximum configurable time is 32s, and the clock source is LSI.

IWDG features register write-protection, which enables and disables WDT by configuring byte, and window mode is selectable.

Reset generates when:

- Reset (if watchdog activated)when the counter value is greater than or equal to the maximum value of the configuration；

6.11.8 Window watchdog (WWDG)

The window watchdog (WWDG) is based on a 6-bit upcounter. It is clocked by PCLK, divide frequency after 4096. The prescaler factor is configurable with options (1/2/4/8/16/32/64/128).

- Reload mode: write a value to a certain register, this value is loaded into counter.
- Window mode: selectable (No enable control. By default, the window value is 0, which indicates the window is invalid)
- Reset conditions (When WDT enable is valid)
  - Reset (if watchdog activated)when the counter value is greater than or equal to the maximum value of the configuration
  - Reset (if watchdog activated)when the counter value is less than the window value
- Interrupt: triggered when the up counter is equal to the maximum value minus 1 (if interrupt enable is configured), which is used to remind system of a coming reset.

6.11.9 SysTick timer

This timer is dedicated to real-time operating systems, but it can also be used as a

standard downcounter.

It has the following Features:

- 24-bit downcounter
- Auto-reload capacity
- Maskable system interrupt generation when the counter reaches 0
- HCLK as Clock source

6.12 Real-time clock (RTC)

The device embeds a RTC and five backup registers. The supply voltage of the RTC is V_{DD}. It has a write protection feature.

Features of the RTC:

- Calendar with subsecond (maximum value configurable), seconds, minutes, hours (24 format)
- Calendar can be initialized
- Reset RTC domain by writing to register
- A Programmable alarm A (any clock within the counter range)
- Outputs of the alarm A and tamper events to pins
- Outputs of a 1Hz clock, OSC32K or XTAL32K to pins
- RTC can wake up system from low-power mode
- Supports alarm interrupt, second interrupt and day interrupt

6.13 Tamper and backup register (TAMP)

Features of the TAMP:

- Five 32-bit backup registers
- Two external tamper detection pins TAMP1/2
- Any tamper detection can erase the backup registers (erase enable configurable)

6.14 Inter-integrated circuit interface (I2C)

The device embeds two I2C peripherals. Refer to Table 6.3 12C features for details.

Features of the I2C:

- Master and slave mode
- Standard mode (up to 100kHz)

- Fast mode (up to 400kHz)
- Super fast mode (up to 1MHz)
- 7-bit addressable mode
- Broadcast call
- Two 7-bit slave addresses (1 with configurable mask)
- Parameters of Master timing configurable
- Optional clock extension
- Software Reset (Register enable is shut down, Internal states machines and the related timing are reset)
- DMA transmission support
- Wakeup from Deepsleep mode on address match

Table 6.3 I2C features

I2C features	I2C1	I2C2
100K, 400K, 1M communication rate support	√	√
7-bit address	√	√
Wakeup from Deepsleep Mode	√	√

6.15 Serial peripheral Interface (SPI)

The device contains two SPI, supporting half-duplex and full-duplex communications. SPI can be configured as master or slave mode. In master mode, clock and chip select signals are generated and output by SPI module, while clock and chip select signals are from external inputs in slave mode. The communication speed is up to 16M in master mode and 8M in slave mode. The data size is configurable from 4-bit to 16-bit to 32-bit.

SPI features programmable clock polarity and phase, the sequence of high bit and low bit to be set, two 32-bit receive/transmit buffer supporting DMA capability, dedicated transmission and reception flags with interrupt capability, overrun flags with interrupt capability in case of master mode fault, SPI bus busy status flag and Hardware CRC support.

6.16 Universal asynchronous receiver transmitter (UART)

The device contains two identical UART modules with independently enabled double buffer receiver/transmitter. It supports half-duplex, full-duplex serial port communications and hardware parity generation and checks. It uses programmable data word length (8 or 9 bits) and configurable 1 or 2 stop bits.

It supports auto baud rate feature and oversampling by 16, with programmable baud rate (15-bit analog-digital divider):adapt common baud rate (2400, 4800, 9600, 19200, 38400,

57600, 115200, 230400).

UART supports continuous communications using DMA. Received/transmitted bytes are buffered in reserved SRAM using DMA.

UART features swappable RX/TX pin configuration whose active level can inverse, p rogrammable data order with MSB-first or LSB (default setting)-first shifting, separate enable bits for receiver/transmitter, separate signal polarity control for transmission and reception, hardware flow control for modem and RS-485 transceiver, communica tion control/error detection flags, interrupt sources with flags and multiprocessor com munications (the device enters mute mode if addresses do not match, wakeup fro m Mute mode when idle frame or address mach is detected).

Parity control:

- Transmit parity bit
- Checks parity of received data byte

Table 6.4 UART features

UART features	UART1/UART2
Hardware flow control for MODEM	√
Continuous communication using DMA	√
Multiprocessor communication	√
Wakeup from Deepsleep mode	√
Idle interrupt	√
Auto baud rate detection	√
RS485 driver enable signal	√

6.17 Serial wire debug port (SW-DP)

An Arm SW-DP interface is provided to allow a serial wire debugging tool to be connected to the MCU.

7 Electrical Characteristics

7.1 Test conditions

Unless otherwise specified, all voltages are referenced to V_{SS}.

7.1.1 Minimum and maximum values

Unless otherwise specified, all minimum and maximum values will be guaranteed at the worst ambient temperature, supply voltage and clock frequency conditions by testing on 100% of the product at ambient temperatures TA=25°C and TA=TAmax (TAmax matches the selected temperature range).

The notes below each table indicate data derived from comprehensive evaluation, design simulation and/or process characteristics and will not be tested on the production line; On the basis of comprehensive evaluation, the minimum and maximum values are obtained by taking the mean value and adding or subtracting three times the standard distribution after the sample test.

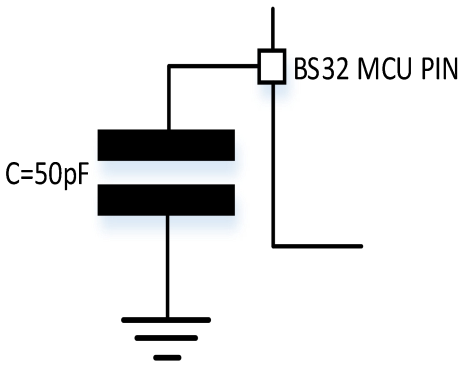
7.1.2 Typical values

Unless otherwise specified, typical data are based on T_A=25°C and V_{DD}=3.3V. This data is for design guidance only and has not been tested.

7.1.3 Load capacitance

The load conditions for measuring pin parameters ara shown in Figure 7.1.

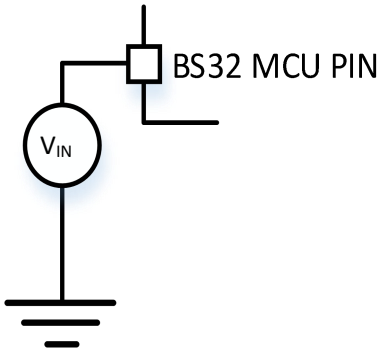
Figure 7.1 Load conditions of ins



7.1.4 Pin input voltage

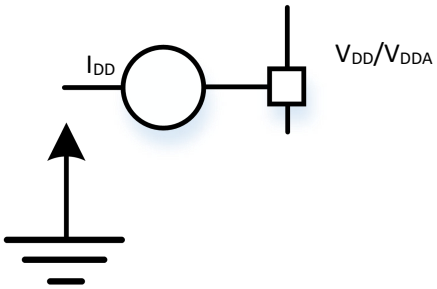
The measurement method of input voltage on the pin is shown in Figure 7.2.

Figure 7.2 Pin input voltage



7.1.5 Current consumption measurement

Figure 7.3 Current consumption measurement



7.2 Absolute maximum rating

If load imposed on the device above the absolute maximum listed in Table 7.1 may cause permanent damage to the device. These are maximum load that can be borne, it does not mean that the functional operation of the device is silent under this condition. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 7.1 Absolute maximum ratings

Symbol	Parameter	Min	Max	Unit
V_{DD}/V_{DDA}	External supply voltage	V_{SSA}-0.3	V_{SSA}+5.5	V
V_{IN}(2)	Input voltage of pin	V_{SS}-0.3	5.5	V
$I_{VDD(PIN)}$	Maximum current into each V_{DD} power pin(source)	-	120	mA
$I_{VSS(PIN)}$	Maximum current out of each V_{SS} ground pin(sink)	-	120	mA
I_{IO}	Output current sunk by any I/O and control pin	-	50	mA
	Output current sourced by any I/O and control pin	-	50	mA
$\Sigma I_{IO(PIN)}$	Total output current sunk by sum of all I/Os and control pins	-	100	mA
	Total output current sourced by sum of all I/Os and control pins	-	100	mA
T_{STG}	Storage temperature range	-40	125	°C
T_J	Maximum junction temperature	-	125	°C

1. The mian power supply (V_{DD}/V_{DDA}) and ground (V_{SS}/V_{SSA}) pins must always be connect to the external power supply within the allowsble range.
2. V_{IN} is not allowed to be greater than V_{IOVCC}.

7.3 General working conditions

Table 7.2 General working conditions

Symbol	Parameter	Min	Max	Unit
f_{HCLK}	AHB clock frequency	0	48	MHZ
f_{PCLK}	APB clock frequency	0	24	MHZ
V_{DD}/V_{DDA}	Supply voltage	2.5	5.5	V
V_{IOVCC}(1)	I/O Supply voltage	2.5	5.5	V
V_{IN}	I/O input voltage	0	V_{IOVCC}	V
T_A	Operating temperature	-40	85	°C
T_J	junction temperature	-40	105	°C

1. V_{IOVCC} equals the input V_{DDA}

7.4 GPIO characteristics

Unless otherwise specified, the parameters given in the table below are derived from tests

performed under ambient temperature and supply voltage conditions summarized in General Operating Conditions. All I/Os are CMOS and TTL compliant.

Table 7.3 GPIO Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
VOH	Output high level voltage for an I/O pin	90	-	-	%IOVCC(1)
VOL	Output low level voltage for an I/O pin	-	-	10	%IOVCC
VIH	Input high level voltage for an I/O pin	70	-	-	%IOVCC
VIL	Input low level voltage for an I/O pin	-	-	30	%IOVCC
Vhys(2)	Standard I/O schmidt trigger voltage hysteresis	10	-	-	%IOVCC
RPU	Pull-up equivalent resistor(3)	-	40	-	KΩ
RPD	Pull-down equivalent resistor	-	40	-	KΩ

1. The hysteresis voltage of the Schmidt trigger switching level. Guaranteed by design, not tested in production.
2. The pull-up and pull-down resistors are designed to be a true resistor in series with a switchable PMOS/NMOS . The resistance ratio of PMOS/NMOS switch is very small.

7.5 Supply current characteristics

Current consumption is a comprehensive indicator of various parameters and factors, including operating voltage, ambient temperature, load on I/O pins, software configuration of the product, operating frequency, flip rate of I/O pins, program position in memory, and executed code.

The current consumption measurements given in each mode in this section are the result of executing a streamlined set of code.

Current consumption of different main frequency/temperature

The microcontroller is under the following conditions:

- AII I/O pins are in push-pull output mode and the output is low.
- All peripherals are closed, unless otherwise specified.
- $f_{PCLK} = f_{HCLK} /2$
- V_{DD}=3.3V

The current consumption test results are shown in Table 7.4.

Table 7.4 Typical current consumption in operation mode, code running in internal flash memory

Parameter	Mode	Conditions	f_{HCLK} (Mhz)	Typ				Unit
				25℃	45℃	65℃	85℃	
IDD	Power supply current in operation mode	PLL=48MHZ, Internal,clock , enable all peripherals,use default clock frequency division	48	13.05	13.26	13.65	14.12	mA
			24	10.72	10.90	11.29	11.80	
			12	9.38	9.57	9.96	10.44	
			6	8.63	8.82	9.23	9.75	
			3	8.18	8.38	8.76	9.25	
IDD	Power supply current in operation mode	PLL=48MHZ, Internal clock,close all peripherals	48	5.90	5.96	6.33	6.8	mA
			24	5.05	5.23	5.64	6.18	
			12	4.35	4.55	4.97	5.50	
			6	3.87	4.07	4.48	6.00	
			3	3.58	3.80	4.22	4.71	

Low power consumption current consumption at room temperature

The microcontroller is under the following conditions:

- AII I/O pins are in push-pull output mode and the output is low.
- All peripherals are closed,unless otherwise specified.
- $f_{PCLK} = f_{HCLK} /2$
- T_A=25℃

The current consumption test results are shown in Table 7.5.

Table 7.5 Typical current consumption in low power mode, code running in internal flash memory

Parameter	Mode	Conditions	VDD（V）	Typ	unit
I_{DD}	deepsleep mode	T_A=25°C BOR off close all peripherals I/O output and pull-down	5.0	6.5	μA
			3.3	6.5	
			2.7	6.1	
			2.6	6.2	
			2.5	6.4	
	shutdown	T_A=25°C BOR off close all peripherals	5.0	3.0	
			3.3	2.1	
			2.7	3.9	
			2.6	1.9	
			2.5	1.9	

Configure current consumption of different wake-up sources

The microcontroller is under the following conditions:

- AII I/O pins (except trigger pins) are in output mode and configured for pull-down.
- All peripherals are closed,unless otherwise specified.
- The working voltage is 3.3V, the working frequency is 48Mhz, the BOR is turned on,and the wake-up PLL timing time is 1ms by default.
- The current consumption test results are show in Table 7.6

Table 7.6 Crrent consumption of configuring different wake-up sources

Parameter	Mode	Wake-up Condition	Before awakening（μA）	After awakening（mA）
I_{DD}	deepsleep	External interrupt EXTI0~15	9.2	5.65
		TIM6 interrupt, clock source LSI	9.2	5.64
		TIM6 interrupt, clock source LSE, oscillation LP structure	12.4	5.82
		TIM6 interrupt,clock source LSE, oscillation HG structure	25	5.82
		TIM6 interrupt, clock source LSI, enable HSE	16	6.19
		RTC interrupt, clock source LSI	9.2	5.72
		RTC interrupt, clock source LSE, oscillation LP structure	12.4	5.76
		UART interrupt	9.5	6.05
		LVDT interrupt	10.5	5.65
		IWDG reset	9.3	5.65
		BOR reset	9.3	5.65
		NRST external reset	9.3	5.74
	shutdown	WKUP pin	4.5	5.53
		RTC interrupt, clock source LSI	4.5	5.53
		RTC interrupt, clock source LSE, oscillation LP structure	7.5	5.75
		RTC interrupt, clock source LSE, oscillation HG structure	50	5.75
		BOR reset	4.5	5.53
		NRST external reset	4.5	5.53

Built-in peripheral current consumption

The microcontroller is under the following conditions:

- AII I/O pins are in output mode and configured for pull-down, except for enabled peripheral I/O ports.
- All peripherals are closed,only enble a peripheral。
- The working voltage is 3.3V, the working frequency is 48Mhz, the BOR is turned on,and the wake-up PLL timing time is 1ms by default.
- f_{HCLK}=48Mhz, fAPB=f_{HCLK}/2, the prescaler coefficient of each peripheral is the default value.

Table 7.7 Current consumption of built-in peripherals

Built-in peripheral	Typical power consumption at 25°C(mA)	Built-in peripheral	Typical power consumption at 25°C(mA)	Built-in peripheral	Typical power consumption at 25°C(mA)
GPIOA	5	TIM14	250	I2C1	120
GPIOB	5	TIM15	430	I2C2	120
GPIOC	5	TIM16	400	SPI1	130
GPIOF	5	TIM17	390	SPI2	130
TIM1	860	UART1	130	IWDG	2
TIM3	540	UART2	130	WWDG	37
TIM6	40	ADC	2700	RTC	2.3

7.6 Internal reset and power manage features

The following parameters are derived from the results of the ambient temperature test and the design criteria.

Table 7.8 Power-on (POR) /Power-down (PDR) reset characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Max
V_{POR}	Power-on threshold	T=-40°C 至 105°C	1.12	1.50	1.92	V
V_{PDR}	Power-down threshold	T=-40°C 至 105°C	0.91	1.24	1.64	V
V_{HSY}	Hysteresis	T=-40°C 至 105°C	0.122	0.263	0.438	V
t_{RST}	Reset timing	T=-40°C 至 105°C	-	3.92	-	ms

Table 7.9 BOR(Brown-out reset) characteristics

Delay_sel	Threshold_sel	PD_Threshold	P0_Threshold	Hysteresis (mV)	Delay_time (us)
BOR0	0	1.902	2.015	113	59.96
	1	1.997	2.103	106	63.83
	2	2.205	2.311	106	72.26
	3	2.496	2.612	116	83.82
	4/5/6/7	2.796	2.907	111	95.3
BOR1	0	1.899	2.015	116	120.1
	1	1.994	2.103	109	128.4
	2	2.201	2.311	110	146.4
	3	2.491	2.612	121	171
	4/5/6/7	2.791	2.907	116	195.3

7.7 Electrical sensitivity characteristics

Based on three different tests (ESD, LU) using specific methods, in order to determine its performance in terms of electrical sensitivity.

Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to all pins of each sample. The sample size depends on the number of supply pins in the device (3 parts×(n+1) supply pins). This test conforms to the ANSI/JEDEC standard.

Table 7.10 ESD absolute maximum ratings

Symbol	Parameter	Conditions	Category	Min	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	T_A=25°C，conforming to ANSI/ESDA/JEDEC JS-001	3B	8000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage （charging equipment model）	T_A=25°C，conforming to ANSI/ESDA/JEDEC JS-002	C2a	750	V

Table 7.11 Static latch-up/Electrical sensitivity

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
LU	I-test	T_A=25°C	-	±200	-	mA
	V_{supply} over voltage		-	8.25	-	V

7.8 External clock source characteristics

The characteristic parameters given in the table below were measured using a high-speed external clock source.

Table 7.12 High-speed external user clock characteristics (HSE)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSE}	User external clock source frequency	-	4	-	20	MHz
C_{HSE}	Recommended load capacitance on OSCIN pin and OSCOUT pin	-	-	-	12(16MHz)	pF
		-	-	-	20(8MHz)	
R_{FHSE}	Feedback resistance	-	-	1	-	MΩ
D_{HSE}	HSE PWM	-	45	50	55	%
I_{DDHSE}	HSE current consumption	V_{DD}=3.3V, T_A=25℃	-	500	-	uA
t_{SUHSE}	Setup time	-	-	3	-	ms

The characteristic parameters given in the table below were measured using a low-speed external clock source.

Table 7.13 Low-speed external user clock characteristics (LSE)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSE}	User external clock source frequency	-	-	32.768K	-	Hz
C_{LSE}	Recommended load capacitance on OSCIN pin and OSCOUT pin	-	-	12.5	-	pF
R_{FLSE}	Feedback resistance	-	-	5	10	MΩ
D_{LSE}	LSE PWM	-	-	50	-	%
I_{DDLSE}	LSE current consumption	SEL=010101 V_{DD}=3.3V, T_A=25℃	-	1.6	-	uA
t_{SULSE}	Setup time	-	-	200	-	ms

7.9 Internal clock source characteristics

The characteristic parameters given in the table below are the data obtained through design simulation and comprehensive test.

High-speed internal (HSI) oscillator

Table 7.14 High-speed internal (HSI) oscillator characteristics

Symbol	Parameter Conditions	Min	Typ	Max	Unit
V_{DD}	Operating voltage	2.5	5	5.5	V
f_{HSI}	frequency VDD=3.3V，TA=27℃	0.994	-	1.006	Mhz
$\Delta temp_{HSI}$	Temperature drift（-40~125℃） Relative 27℃，2.5V≤VDD≤5.5V	-1.8	-	1.3	%
ΔVDD_{HSI}	Pressure drift （2.5~5.5V） Relative 3.3V，-40~125℃	-0.6	-	0.08	%
$I_{DD(HSI)}$	HSI oscillator power consumption(1)	-	93.5	-	μA

1.Guaranteed by design,not tested in production.

Low-speed internal (LSI) oscillator

Table 7.15 Low-speed relatived internal (LSI) oscillator characteristics

Symbol	Parameter Conditions	Min	Typ	Max	Unit
V_{DD}	Operating voltage	2.5	5	5.5	V
f_{LSI}	frequency VDD=3.3V，TA=27℃	32	-	34	Khz
$\Delta temp_{LSI}$	Temperature drift（-40~125℃） Relative 27℃，2.5V≤VDD≤5.5V	-0.9	-	2.5	%
ΔVDD_{LSI}	Pressure drift（2.5~5.5V） Relative 3.3V，-40~125℃	-0.7	-	0.8	%
$I_{DD(LSI)}$	LSI oscillator power consumption	-	1.83(1)	-	μA

1. When V_{DD}=3.3V, the typical value of IDD(LSI) is1.21μA.

7.10 PLL Characteristics

The characteristic parameters given in the table below are the data obtained through design simulation and comprehensive test.

Table 7.16 PLL characteristics

Symbol	Parameter	Min	Typ	Max	Unit
V_{DD}	Operating voltage	2.5	5	5.5	V
Temp	Temperature	-40	25	125	℃
f_{PLL_IN}	Input clock	-	1	-	Mhz
f_{PLL_OUT}	PLL frequency doubling output clock	-	48	-	Mhz
$t_{su(PLL)}$	PLL startup time	51.17	66.2	118.2	μs
$I_{DD(PLL)}$	PLL power consumption	158.7	315.3	402.1	μA
Jitter	Jitter（peak-to-pesk value）	6.609	30.3	53.66	ps

7.11 FLASH memory characteristics

The characteristic parameters given in the following table are guaranteed by design, not tested in production.

Table 7.17 FLASH memory characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
N_{END}	Endurance	T_A= -40℃ ~ 105℃	100			kcycles
t_{RET}	Data retention	T_A= 105℃	10	-	-	years
t_{PROG}	Byte program time	T_A= -40℃ ~ 85℃	48.55	50.75	-	us
t_{ERASE}	Page erase time	T_A= -40℃ ~ 85℃ Repeat page erase mode	1	1.25	-	ms
		T_A= -40℃ ~ 85℃ Monopulse page erase mode	4	4.5	-	
t_{MERASE}	Block erase time	T_A= -40℃ ~ 85℃	8	10	-	ms

7.12 ADC characteristics

Unless otherwise specified, the parameters in the table below are measured using the required ambient temperature, clock frequency, and V_{DDA} supply voltage.

Table 7.18 ADC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	input voltage	-	2.5	3.3	5.5	V
V_{IN}	ADC input voltage	Single-ended input mode	V_{SSA}	-	V_{DDA}	V
$I_{DD(ADC)}$	ADC operating current	V_{DDA}=3.3V, T_A=25℃, Bias current 15uA	-	2.9	-	mA
I_{ADCIN}	ADC input current	V_{DDA}=3.3V, T_A=25℃	-	-	1	μA
f_{ADC}	ADC clock frequency	-	1.5	24	30	Mhz
f_S	ADC sampling conversion rate	V_{DDA}=5V, T_A=25℃, Bias current 15uA	-	-	1	MSPS

t_S	ADC sampling time	-	3	-	1024	$1/f_{ADC}$

Table 7.18 ADC characteristics(continue)

t_{CONV}	ADC Total conversion time (sampling+interval+conversion)	Resolution 12 bits	21~1042			$1/f_{ADC}$
R_S	ADC input switch equivalent resistance	RC filtering	-	1.2	-	KΩ
		No RC filtering	-	2.3	-	
ADC_{RESO}	Resolution	-	12			Bit
ENOB	Actual significant.digit	V_{DDA}=3.3V, TA=25℃	9.5	10	-	Bit
DNL	Differential nonlinearity	2.5V≤V_{DDA}≤ 5.5V, TA=25℃	-	-	±1.5	LSB
INL	Integral nonlinearity		-	-	±2	LSB
EO	Misalignment error		-	-	±2.5	LSB
EG	Gain error		-	-	±2	LSB
EF	Full scale error		-	-	±4	LSB
SNDR	Signal-to-noise distortion ratio	2.5V≤V_{DDA}≤ 5.5V, 40Khz-0.02dBFS	66	-	-	dB
THD	Total harmonic distortion		-	-	-72	dB

1. Unless otherwise specified, typical values are measured at TA = 25℃.

ADC power consumption in different bias current configurations

The microcontroller has the following conditions:

T_A=25℃. The channel pin is externally with a 10K sliding rheostat, which controls the input voltage of ADC channel at 2.5V and changes the bias current to measure the current consumption of MCU under the condition of ADC.

ADC configuration status：12bitresolution、the sampling comparison interval is 0、the sampling conversion interval is 0、the sampling time is set to the maximum.

The current consumption test results are shown in the following table：

Table 7.19 ADC bias current and current consumption

Operating voltage	Bias current	Power consumption (mA)	Operating voltage	Bias current	Power consumption (mA)
	OPAMP_5UA + COMP_12UA	3.84		OPAMP_5UA + COMP_12UA	3.7
	OPAMP_5UA + COMP_10UA	3.3		OPAMP_5UA + COMP_10UA	3.13
	OPAMP_5UA + COMP_9UA	3.08		OPAMP_5UA + COMP_9UA	2.9
	OPAMP_5UA + COMP_7UA	2.68		OPAMP_5UA + COMP_7UA	2.41
	OPAMP_5UA + COMP_5UA	2.2		OPAMP_5UA + COMP_5UA	1.85

3.3V	OPAMP_5UA + COMP_4UA	1.96	5V	OPAMP_5UA + COMP_4UA	1.61
	OPAMP_5UA + COMP_2UA	1.46		OPAMP_5UA + COMP_2UA	1.05
	OPAMP_4UA + COMP_12UA	3.74		OPAMP_4UA + COMP_12UA	3.67
	OPAMP_4UA + COMP_10UA	3.29		OPAMP_4UA + COMP_10UA	3.13
	OPAMP_4UA + COMP_9UA	3.07		OPAMP_4UA + COMP_9UA	2.88
	OPAMP_4UA + COMP_7UA	2.59		OPAMP_4UA + COMP_7UA	2.33
	OPAMP_4UA + COMP_5UA	2.1		OPAMP_4UA + COMP_5UA	1.77
	OPAMP_4UA + COMP_4UA	1.86		OPAMP_4UA + COMP_4UA	1.51
	OPAMP_4UA + COMP_2UA	1.37		OPAMP_4UA + COMP_2UA	0.95
	OPAMP_3UA + COMP_12UA	3.65		OPAMP_3UA + COMP_12UA	3.6
	OPAMP_3UA + COMP_10UA	3.19		OPAMP_3UA + COMP_10UA	3.06
	OPAMP_3UA + COMP_9UA	2.98		OPAMP_3UA + COMP_9UA	2.82
	OPAMP_3UA + COMP_7UA	2.51		OPAMP_3UA + COMP_7UA	2.26
	OPAMP_3UA + COMP_5UA	2.02		OPAMP_3UA + COMP_5UA	1.7
	OPAMP_3UA + COMP_4UA	1.79		OPAMP_3UA + COMP_4UA	1.44
	OPAMP_3UA + COMP_2UA	1.28		OPAMP_3UA + COMP_2UA	0.88
	OPAMP_2UA + COMP_12UA	3.56		OPAMP_2UA + COMP_12UA	3.5
	OPAMP_2UA + COMP_10UA	3.12		OPAMP_2UA + COMP_10UA	2.97
	OPAMP_2UA + COMP_9UA	2.89		OPAMP_2UA + COMP_9UA	2.72
	OPAMP_2UA + COMP_7UA	2.42		OPAMP_2UA + COMP_7UA	2.15
	OPAMP_2UA + COMP_5UA	1.92		OPAMP_2UA + COMP_5UA	1.6
	OPAMP_2UA + COMP_4UA	1.69		OPAMP_2UA + COMP_4UA	1.34
	OPAMP_2UA + COMP_2UA	1.25		OPAMP_2UA + COMP_2UA	0.78

7.13 Standard SPI characteristics

Unless otherwise specified, the parameters in the table below are measured satisfactory the required ambient temperature, clock frequency, and V_{DDA} supply voltage.

Table 7.20 Standard SPI characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{SCK}	SCK clock frequency	Master mode	-	-	16	MHz
		Slave mode	-	-	8	
$t_{SCK(H)}$	SCK high time	-	31	-	-	ns

$t_{SCK(L)}$	SCK low time	-	31	-	60	ns
$t_{V(MO)}$(1)	Master data output valid time	After enable	-	-	-	ns
$t_{H(MO)}$(1)	Master data output hold time	After enable	2	-	-	ns
$t_{SU(MI)}$(1)	Master input setup time	-	5	-	-	ns
$t_{H(MI)}$(1)	Master input hold time	-	5	-	-	ns
$t_{SU(NSS)}$(	NSS enable setup time	Slave mode	125	-	-	ns
$t_{H(NSS)}$(1)	NSS enable hold time	Slave mode	62	-	-	ns
$t_{A(SO)}$(1)	Slave data output arrive time	-	-	-	38	ns
$t_{DIS(SO)}$(1	Slave data output disappear	-	3	-	10	ns
$t_{V(SO)}$(1)	Slave data output valid time	After enable	-	-	120	ns
$t_{H(SO)}$(1)	Slave data output hold time	After enable	15	-	-	ns
$t_{SU(SI)}$(1)	Slave data input setup time	-	5	-	-	ns
$t_{H(SI)}$(1)	Slave data input hold time	-	4	-	-	ns

1. Derived from comprehensive evaluation, not tested in production.

7.14 IIC characteristics

Unless otherwise specified, the parameters in the table below are measured satisfactory the required ambient temperature, clock frequency, and V_{DD} supply voltage.

Table 7.21 IIC Interface characteristics

Symbol	Parameter	conditions	Standard mode		Fast mode		Super fast mode		Unit
			Min	Max	Min	Max	Min	Max	
f_{SCL}	SCL clock frequency	T_A=25℃	-	100 K	-	400 K	-	1M	Hz
$t_{SCL(H)}$	SCL high time		4.0	-	0.6	-	0.3	-	us
$t_{SCL(L)}$	SCL low time		4.7	-	1.3	-	0.7	-	us

7.15 Embedded reference voltage characteristics

The characteristic parameters given in the table below are the data obtained through design simulation and comprehensive test.

Table 7.22 Embedded internal reference voltage characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{REFINT}	Internal reference voltage	-40℃< T_A < 105℃, 2.5V≤V_{DDA}≤5.5V	1.183	1.214	1.241	V

$t_{S\_VREFINT}$(1)	ADC sampling time when reading the internal reference voltage	-	3	-	-	us
ΔV_{REFINT}(1)	Internal reference voltage distribution over temperature	-40℃< T_A < 105℃, V_{DDA} =3V	1.184	1.213	1.228	mV
T_{coeff}(1)	Temperature coefficient	-	22.88	23.36	61.77	ppm/℃
T_{start}(1)	Startup time	-	47.99	65.99	82.41	us

1. Guaranteed by design,not verified in production

Table 7.23 Internal reference voltage calibration value

Symbol	Parameter	Memory address
V_{REFINT_CAL}	Adjut the internal reference voltage after calibration T_A=25℃, V_{DDA}=3.3V	0x0002 0380

7.16 Embedded temperature sensor characteristics

The characteristic parameters given in the table below are the data obtained through design simulation and comprehensive test.

Table 7.24 Embedded TS characteristics

Symbol	Parameter	Min	Typ	Max	Unit
Avg_Slope(1)	Average slope	3.12	3.206	3.237	mV/℃
V_{25}	Voltage at 25℃	951.2	964.4	976.1	mV
V_{27}	Voltage at 27℃	957.5	970.8	982.6	mV
T_{START}(1)	Startup time	3.876	7.709	12.97	us
T_{S_TEMP}(1)	ADC sampling time when reading the temperature	3	-	-	us

1. Guaranteed by design, not tested in production.

8 Package Information

BYD semiconductor offers various packaging forms according to different environments,to meet the needs of different scenarios. Currently, LQFP48, LQFP32, QFN32 are available. Consult the packaging manufacturer for specific packaging information.

8.1 LQFP48 package information

LQFP48 is a 48-pin, 7 x 7 mm low-profile quad flat package.

Figure 8.1 LQFP48 package outline

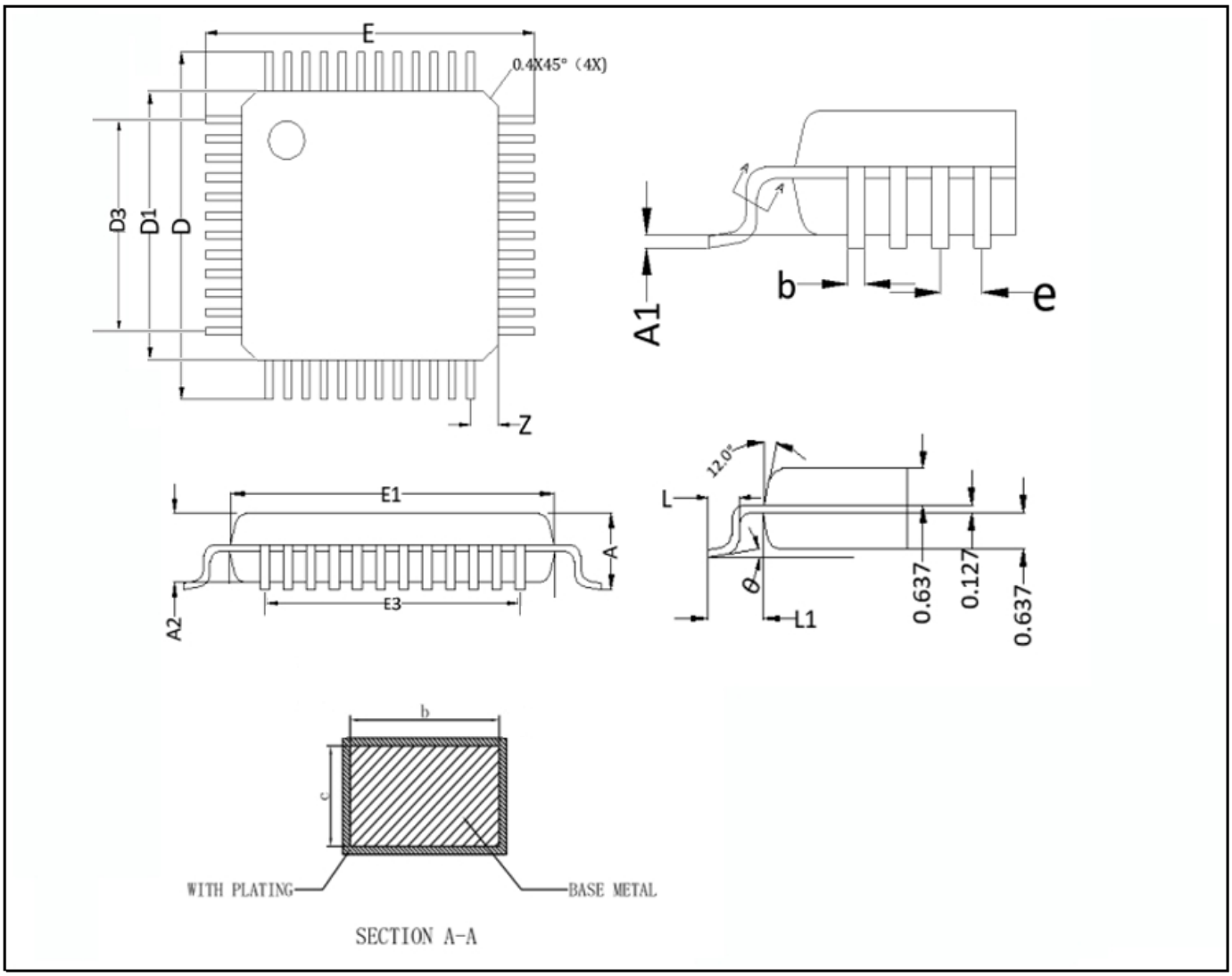


Table 8.1 LQFP48 mechanical data

Symbol	millimeters			inches		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.60	-	-	0.0630
A1	0.05	-	0.15	0.0020	-	0.0059
A2	1.35	1.40	1.45	0.0531	0.0551	0.0571
b	0.18	-	0.27	0.0071	-	0.0106
c	0.13	-	0.18	0.0051	-	0.0070
D	8.80	9.00	9.20	0.3465	0.3543	0.3622
D1	6.90	7.00	7.10	0.2717	0.2756	0.2795
D3	5.50BSC			0.2165BSC		
E	8.80	9.00	9.20	0.3465	0.3543	0.3622
E1	6.90	7.00	7.10	0.2717	0.2756	0.2795
E3	5.50BSC			0.2165BSC		
e	0.50BSC			0.0197BSC		
L	0.45	0.60	0.75	0.0177	0.0236	0.0295
L1	1.00REF			0.0394REF		
θ	0°	3.5°	7°	0°	3.5°	7°

1. The value of inch is rounded based on the data in millimeters and converted to 4 decimal places.

8.2 LQFP32 package information

LQFP32 is a 32-pin, 7 x 7 mm low-profile quad flat package.

Figure 8.2 LQFP32 package outline

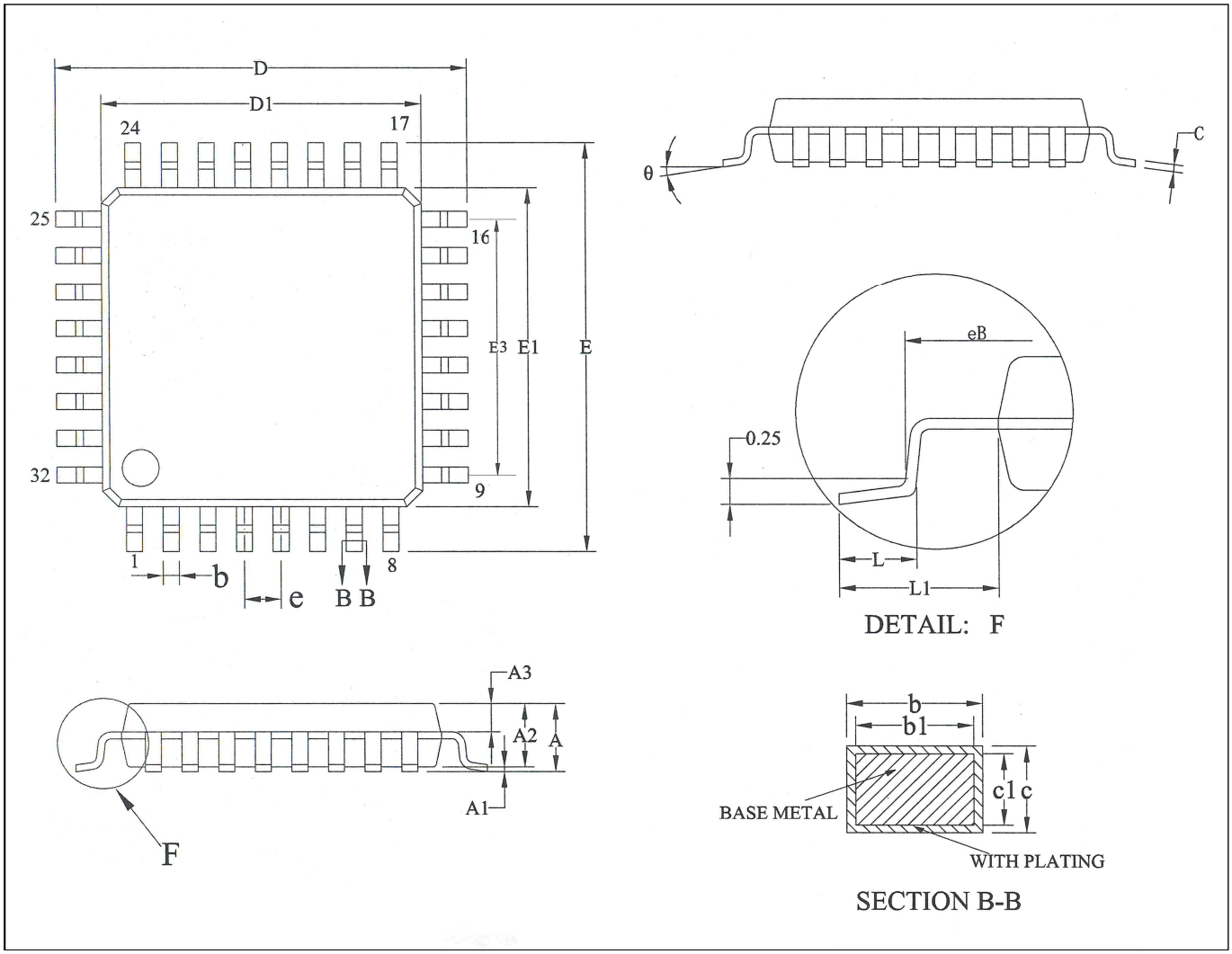


Table 8.2 LQFP32 mechanical data

Symbol	millimeters			inches		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.60	-	-	0.0630
A1	0.05	-	0.15	0.0020	-	0.0059
A2	1.35	1.40	1.45	0.0531	0.0551	0.0571
A3	0.59	0.64	0.69	0.0232	0.0252	0.0272
b	0.32	-	0.43	0.0126	-	0.0169
c	0.13	-	0.18	0.0051	-	0.0070
D	8.80	9.00	9.20	0.3465	0.3543	0.3622
D1	6.90	7.00	7.10	0.2717	0.2756	0.2795
E	8.80	9.00	9.20	0.3465	0.3543	0.3622
E1	6.90	7.00	7.10	0.2717	0.2756	0.2795
E3	5.60BSC			0.2205BSC		
e	0.80BSC			0.0315BSC		
L	0.45	0.60	0.75	0.0177	0.0236	0.0295
L1	1.00REF			0.0394REF		
θ	0°	3.5°	7°	0°	3.5°	7°

1. The value of inch is rounded based on the data in millimeters and converted to 4 decimal places.

8.3 QFN32 package information

QFN32 is a 32-pin, 5 x 5 mm low-profile quad flat package..

Figure 8.3 QFN32 package outline

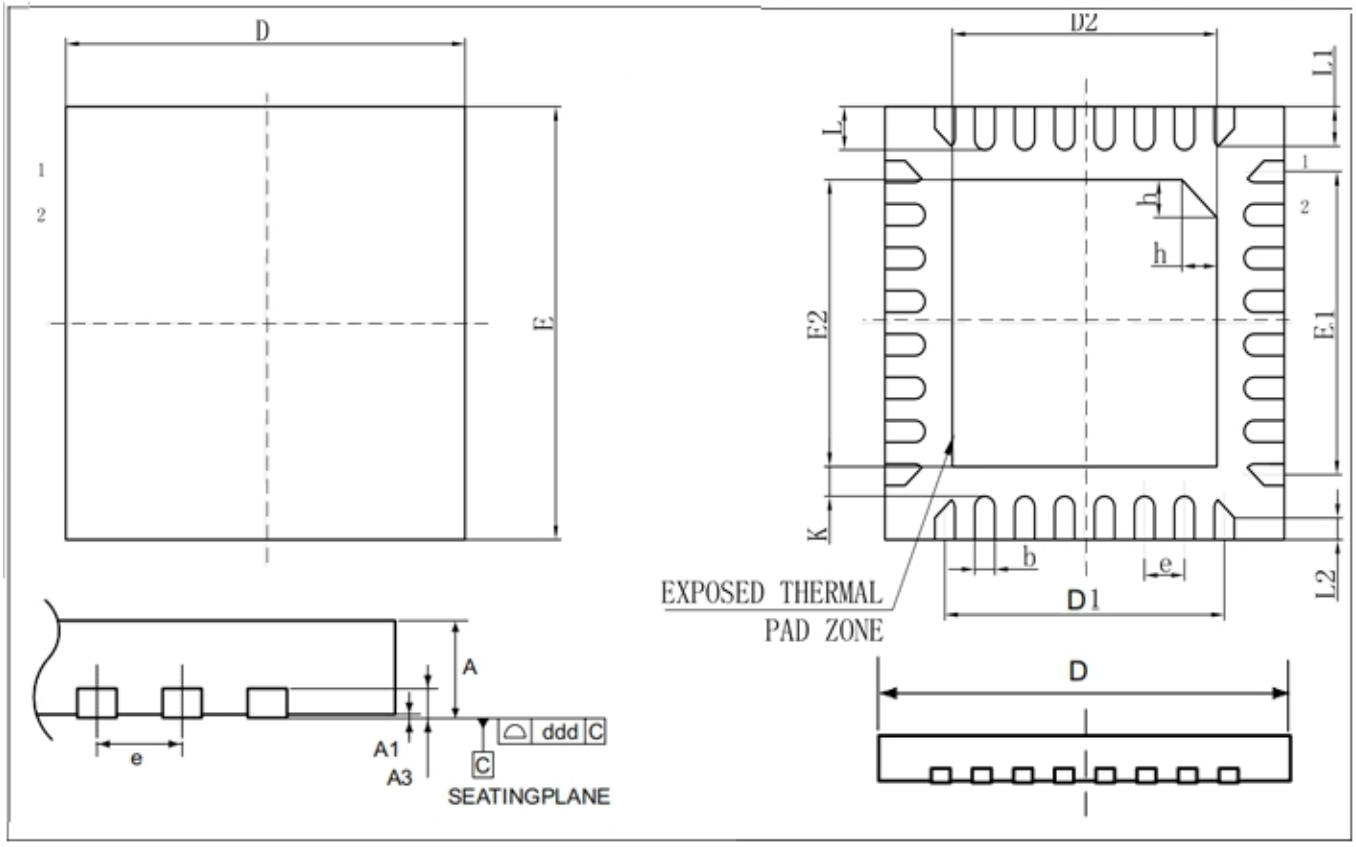


Table 8.3 QFN32 mechanical data

Symbol	millimeters			inches		
	Min	Typ	Max	Min	Typ	Max
A	0.50	0.55	0.60	0.0197	0.0217	0.0236
A1	0	0.02	0.05	0	0.0008	0.0020
A3		0.15REF			0.0059REF	
b	0.18	0.23	0.28	0.0071	0.0091	0.0110
D	4.90	5.00	5.10	0.1929	0.1969	0.2008
D1		3.50BSC			0.1378BSC	
D2	3.40	3.50	3.60	0.1339	0.1378	0.1417
E	4.90	5.00	5.10	0.1929	0.1969	0.2008
E1		3.50BSC			0.1378BSC	
E2	3.40	3.50	3.60	0.1339	0.1378	0.1417
e		0.50BSC			0.0197BSC	
L	0.30	0.40	0.50	0.0118	0.0157	0.0197
ddd	-	-	0.08	-	-	0.0031

1. The value of inch is rounded based on the data in millimeters and converted to 4 decimal places.

8.4 Attention

1. **Chip validity: 1 year under vacuum sealed package**
2. **Baking requirements: the products must be baked at high temperature (125℃ bake 8H) before going online, and the unused products must be baked at high temperature (125℃ bake 8H) before going online.**
3. **Storage environment: constant temperature and humidity 20±5℃ humidity 30%-60%(vacuum sealed package)**
4. **Humidity sensitivity level: MSL3 requires that it should be used online within 168 hours after unpacking**

9 Packing Information

9.1 Tray

With desiccant,humidity indicator card,put into an anti_static bag,and vacuum

9.2 Packing quantity

Table 9.1 packing information

Package form	Piece/Plate	Plate/pack	Piece/pack	Pack/Box	Piece/Box	Packaging method
LQFP48	250	10	2500	6	15000	Tray
LQFP32	250	10	2500	6	15000	Tray
QFN32	490	10	4900	6	29400	Tray

10 Ordering Information

Example BS32 F 030 x B x 6

Device series

BS32 = BYD Semiconductor 32-bit microcontroller

Device type

F = general-purpose

Sub-series

030 = Cortex-M0+ economical configuration

Pin count

F = 20

K = 32

C = 48

R = 64

Flash memory size

4 = 16 KB

6 = 32 KB

8 = 64 KB

B = 128 KB

C = 256 KB

Package type

P = TSSOP

T = LQFP

U = QFN

Ambient temperature range

- 40℃ ~ 85℃

11 Revision History

Table 10.1 Revision history

Version	Data	Description
V1.0.0	09/11/2022	1.Initial release
V1.0.1	23/11/2022	1.Updated electrical characteristics content
V1.0.2	22/12/2022	1. Updated electrical characteristics content 2. Add information of packing
V1.0.3	17/03/2023	1. Updated electrical characteristics content 2. Updated package information

12 Terminology

The comparison of some technical terms in the document and the actual application process is shown in Table 11.1 technical terms comparison table.

Table 11.1 Terminology List

Terminology	Definition
ADC	Analog-digital converter
AHB	Advanced high-performance bus
APB	Advanced peripheral bus
CRC	Cyclic redundancy check calculation unit
DMA	Direct memory access
ESD	Electro-Static discharge
EXTI	Extended interrupt/event controller
FLASH	Flash memory
GPIO	General-purpose input/output
HSE	High-speed external clock
HSI	High speed internal clock
I2C	Inter-integrated circuit interface
IWDG	Independent watchdog
LSE	Low-speed external clock
LSI	Low-speed internal clock
NVIC	Nested vectored interrupt controller
PDR	Power-down reset
PLL	Phase locked loop
POR	Power-on reset
RAM	Random access memory
RTC	Real-time clock
SPI	Serial peripheral interface
SRAM	Static random access memory
SW-DP	Serial wire debug port
TAMP	Tamper
TIM	Timer
TS	Temperature sensor
UART	Universal asynchronous receiver/transmitter
WWDG	Window watchdog

Disclaimer

- The information contained herein is subject to change without notice.
- **BYD Semiconductor Company Limited** will ensure the high quality and stability of products. However, due to the inherent characteristics of general semiconductor devices such as electrical sensitivity and susceptibility to external physical damage,Our products may fail or fail under these circumstances.It is the user's liability to design a safe and stable system following the safety requirements when using BYD products. User can take measures to avoid the possible accidents, fire and public injuries by the removal of the extra devices, failure and fire prevention. When using the products, please make sure to follow the operation steps specified in the company's latest manual to use the product.
- The products listed in this document are intended for use in general electronics applications (computer, **p**ersonal equipment, office equipment, measuring equipment, industrial robotics, domestic appliances, etc.). However, the products are not suitable for use in particular devices that require ultra-high stability and quality, which may result in personal injury or death. ("Unexpected use")The products cannot be applied to atomic energy control equipment, aircraft and aviation devices, transportation equipment, traffic signal equipment, combustion control equipment, medical equipment and all safety equipment. The company will not be responsible for the loss and injury caused by the user' use in the non-product application scope listed above.