1. BF7812AMXX-XJLX MCU General Description

1.1. Features

- **Core: 1T 8051**
  - Operating frequency: 12MHz, 6MHz, 4MHz, 1MHz
  - Clock error: ±1% @ -20℃ ~65℃, 5V
    ±3% @ -40℃ ~105℃, 5V
- **Memory (FLASH)**
  - CODE: 15.5K bytes
  - DATA: 512 bytes
  - SRAM: 256 bytes(data)+512 bytes(xdata)
  - Support 4K BOOT function
- **Clock source, reset and power management**
  - Internal low-speed clock LIRC: 32kHz
    Clock error: ±20% @25℃, 5V
    ±35% @-40℃ ~105℃, 5V
  - Internal high-speed RC oscillator: 1MHz
  - External crystal oscillator: 32768Hz/4MHz
  - 8 resets, including brown-out reset voltage: 2.8V/3.3V/3.7V/4.2V
  - Low voltage detection: 3.0V/3.3V/3.6V/3.9V/4.2V
- **IO**
  - PB0~PB7: built-in pull-up/pull-down resistors 30k, other IOs: built-in pull-up resistors 4.7k
  - High current sink port (PB0~PB7)
  - Support IO function remapping
  - All IO ports support external interrupt function, INT0~2 (rising-edge, falling-edge, doub-edge), INT3 shared interrupt source (rising-edge, falling-edge)
- **Communication module**
  - 2*UART communication, support IO mapping
  - IIC slave mode, support 100/400kHz
- **12-bit PWM**
  - PWM0 supports 1 channel output
  - PWM1 supports 2 channels, the same period and duty cycle, configurable polarity
- **Operating voltage: 2.7V ~ 5.5V**
- **Operating temperature: -40℃ ~ 105℃**
  - Enhanced industrial grade, in line with JESD industrial grade reliability certification standards
- **12-bit high-speed ADC**
  - Up to 26 analog input channels
- **Interrupt**
  - Two-level interrupt priority capablity
  - ADC, CSD, LED, INT0/1/2/3, LVDT, Timer0~2, WDT, UART0/1, IIC interrupt
- **Timer**
  - 16-bit Timer0/1/2
  - Timer2 clock source is internal low-speed clock LIRC 32k or XTAL 32768Hz/4MHz
  - Watchdog timer, overflow time 18ms to 2.304s
- **LED driver**
  - Support 4x4, 4x5, 5x6, 6x7, 7x7, 7x8, 8x8 dot matrix driver
  - LED0~LED8 scan sequence is configurable
- **Low power management**
  - Idle mode 0 and Idle mode 1
  - Idle mode 1, power consumption 10μA @5V typical
- **CTK**
  - The key sensitivity is set independently
  - Capacitive keys can be reused as GPIO
- **Two-wire programming, single-wire debugging simulation interface**
- **Package**
  - TSSOP20/TSSOP28/SOP20/SOP28

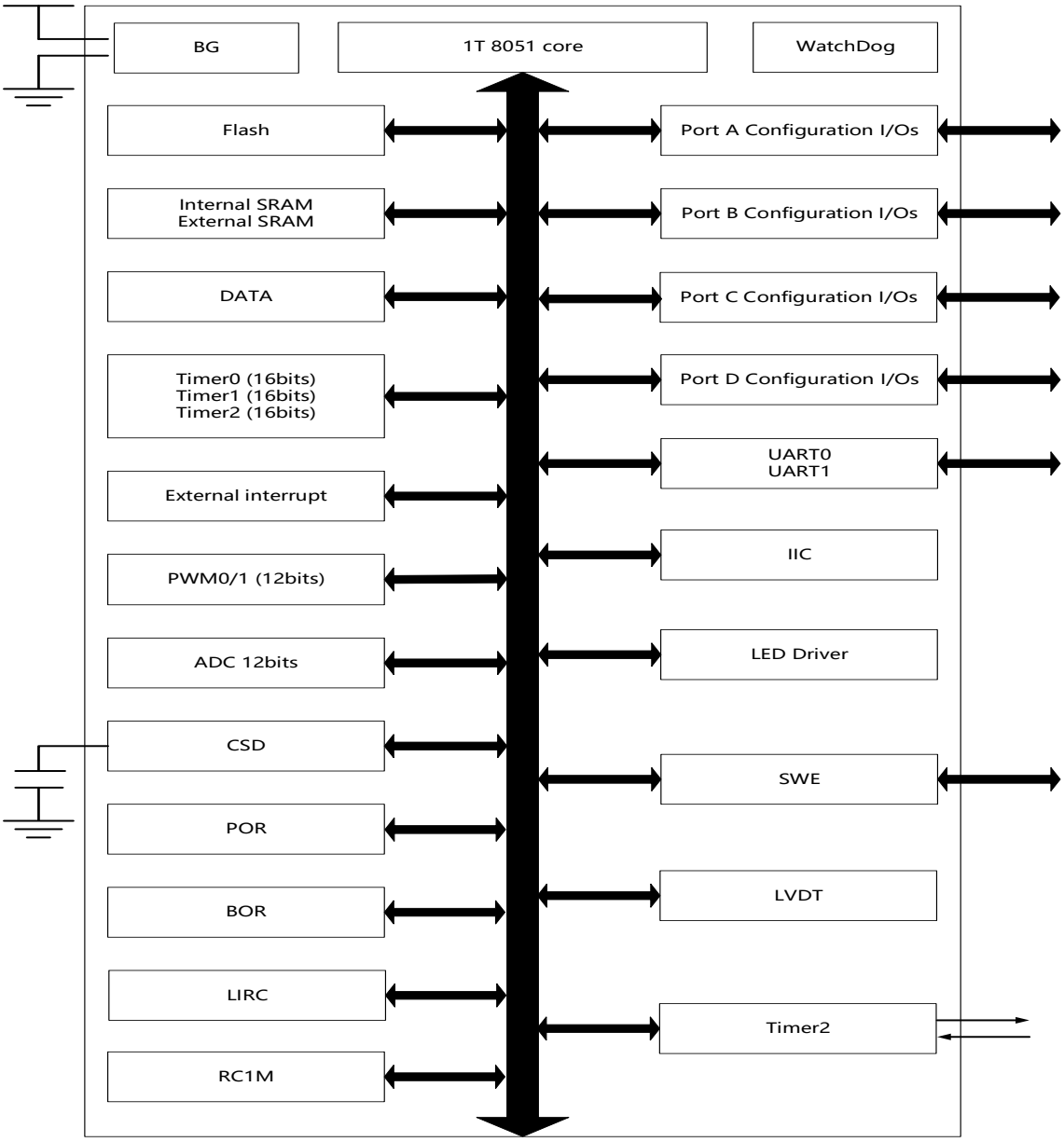
1.2. Overview

The BF7812AMXX-XJLX uses the high speed 8051 core with 1T instruction cycle, compared to the standard 8051 (12T) instruction cycle, has the quicker running speed, compatibility standard 8051 instruction.

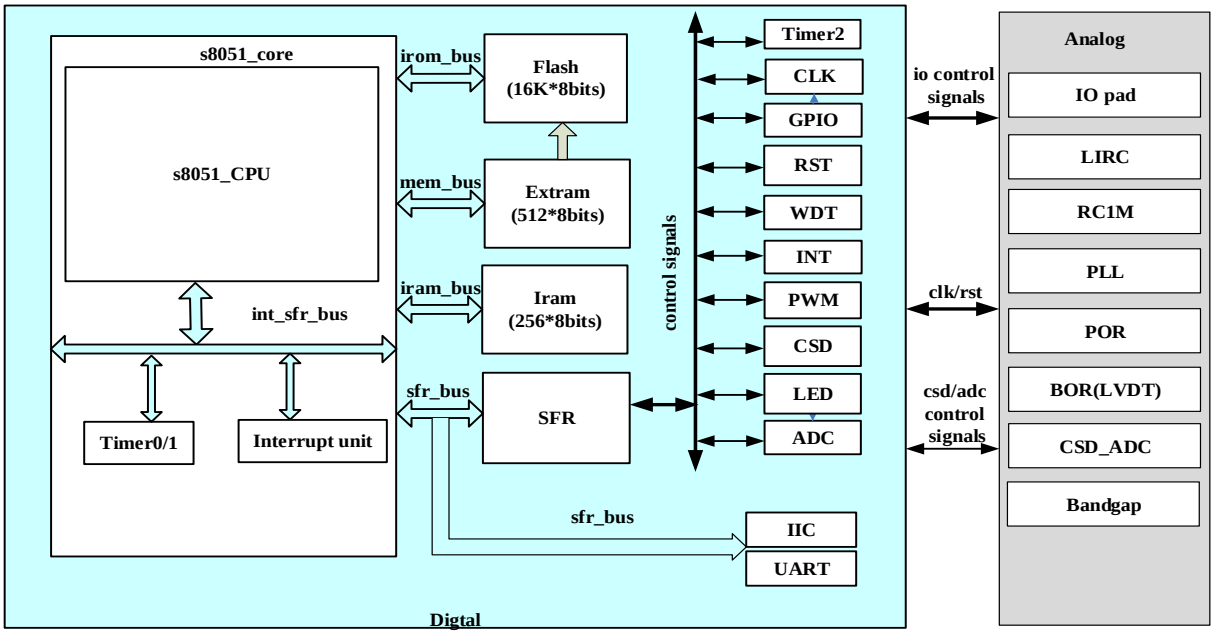
The BF7812AMXX-XJLX includes a watchdog, key detection, LED serial dot matrix driver, IIC, UART, low voltage detection, power down reset, 12-bit PWM, Timer0, Timer1, Timer2, 12-bit successive approximation ADC, low power management, etc.

The BF7812AMXX-XJLX integrates multiple capacitive detection channels, which can be used for proximity sensing or touch detection. Each channel can be flexibly configured to achieve various applications such as keys, wheels, sliders, etc., and each channel can adjust the touch sensitivity through the corresponding function register.

1.3. System Architecture

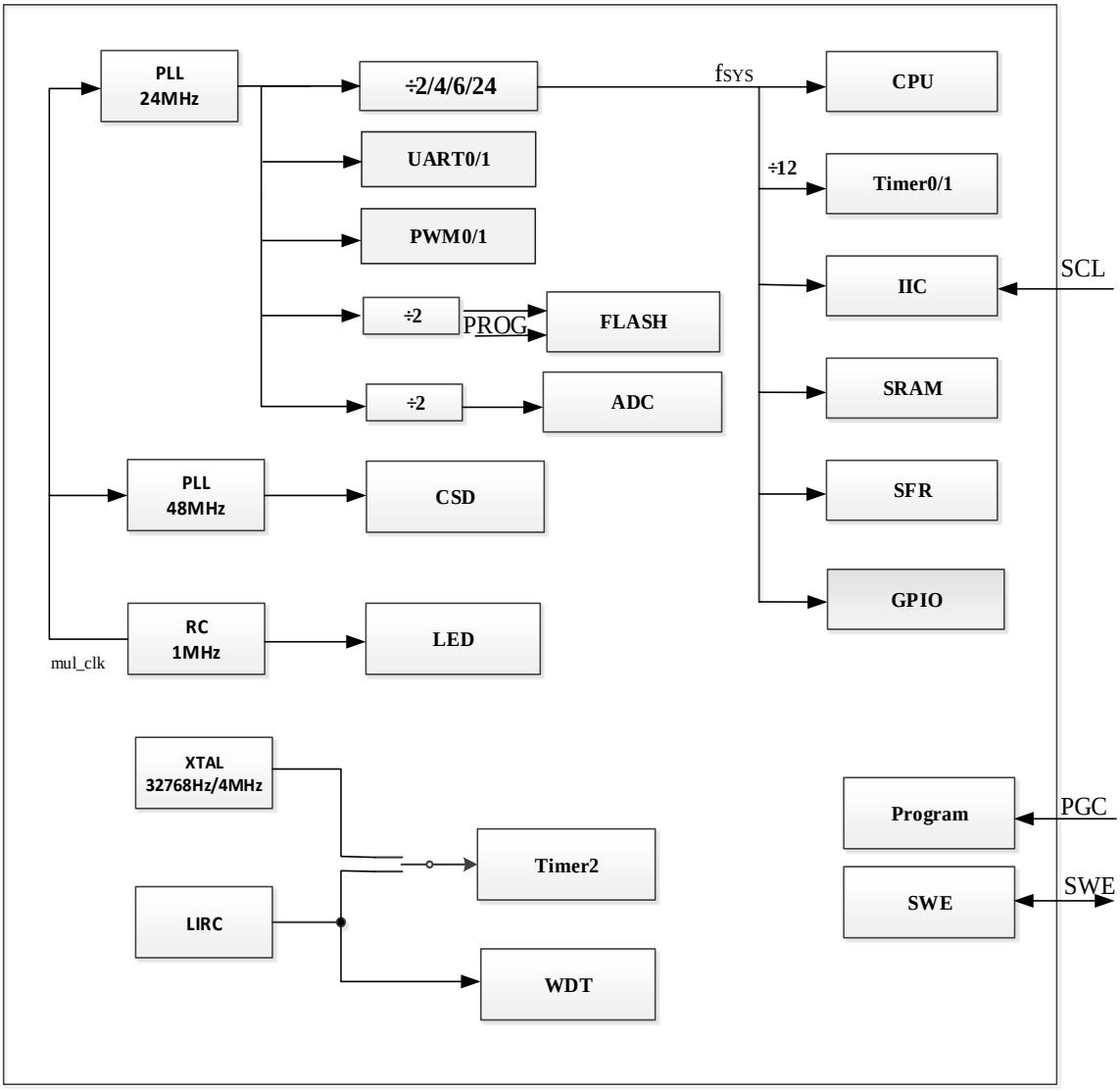


System architecture



System bus frame diagram

1.4. Clock Diagram



Clock Diagram

1.5. Selection List

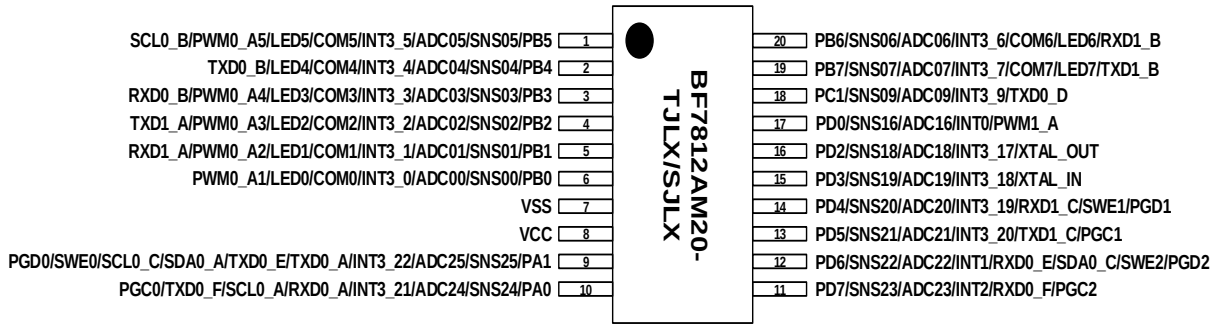
Type		BF7812AM20-TJLX/SJLX	BF7812AM28-TJLX/SJLX
Operating voltage (V)		2.7~5.5	2.7~5.5
Operating frequency (Hz)		12M	12M
Core		1T 8051	1T 8051
Memory (Bytes)	CODE	15.5/11.5K	15.5/11.5K
	BOOT	0/4K	0/4K
	DATA	512	512
	SRAM	256+512	256+512
Timer	WDT	1	1
	Timer0*16bit	1	1
	Timer1*16bit	1	1
	Timer2*16bit	1	1
Communication module	IIC	1	1
	UART	2	2
Analog module	ADC*12bit	18	26
GPIO		18	26
KEY		18	26
COM		8	8
INT		18	26
Display module	LED serial	7*8	8*8
PWM module	PWM0*12bit	1	1
	PWM1*12bit	1	2
Package		TSSOP20/SOP20	TSSOP28/SOP28

Selection list

Note: The space size of CODE area + BOOT area is 15.5K Bytes.

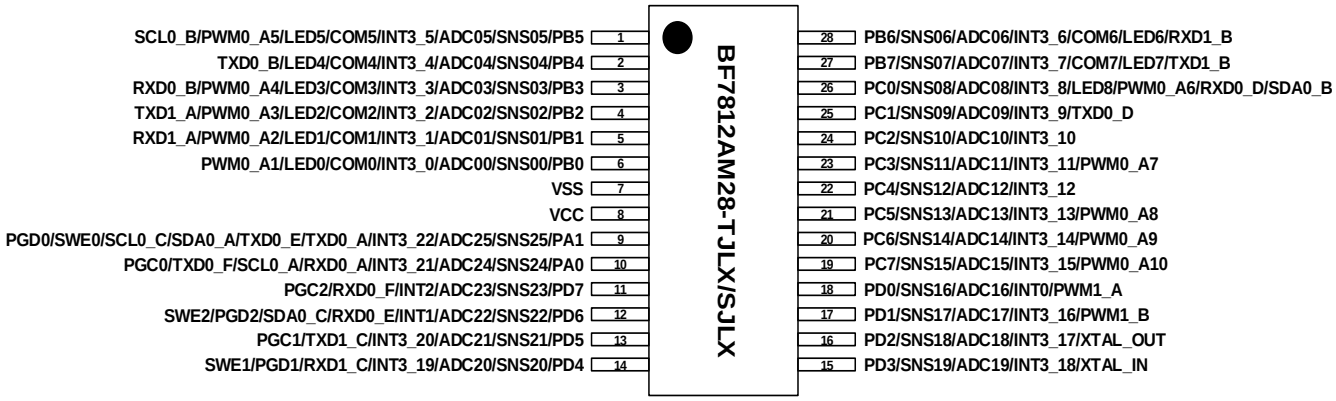
1.6. Pin Assignment

1.6.1. TSSOP20/SOP20



BF7812AM20-TJLX/SJLX Pin Diagram

1.6.2. TSSOP28/SOP28



BF7812AM28-TJLX/SJLX Pin Diagram

1.7. Pin Description

BF7812AM28-TJLX/SJLX	BF7812AM20-TJLX/SJLX	Function description
1	1	Default function: GPIO <PB5> other functions: SNS05: Touch key channel 5 ADC05: ADC channel 05 INT3_5: External Interrupt 3_5 COM5: Large current sink port LED5: LED serial dot matrix PWM0_A5: PWM0_A5 Output port SCL0_B: Serial clock line of IIC
2	2	Default function: GPIO <PB4> other functions: SNS04: Touch key channel 4 ADC04: ADC channel 04 INT3_4: External Interrupt 3_4 LED4: LED serial dot matrix COM4: Large current sink port TXD0_B: Serial port send
3	3	Default function: GPIO <PB3> other functions: SNS3: Touch key channel3 ADC03: ADC channel 03 INT3_3: External Interrupt 3_3 LED3: LED serial dot matrix COM3: Large current sink port PWM0_A4: PWM0_A4 Output port RXD0_B: Serial port receiving
4	4	Default function: GPIO <PB2> other functions: SNS02: Touch key channel 2 ADC02: ADC channel 02 INT3_2: External Interrupt 3_2 LED2: LED serial dot matrix COM2: Large current sink port PWM0_A3: PWM0_A3 Output port

		TXD1_A: Serial port send
5	5	Default function: GPIO <PB1> other functions: SNS01: Touch key channel 1 ADC01: ADC channel 01 INT3_1: External Interrupt 3_1 LED1: LED serial dot matrix COM1: Large current sink port PWM0_A2: PWM0_A2 Output port RXD1_A: Serial port receiving
6	6	Default function: GPIO <PB0> other functions: SNS00: Touch key channel 0 ADC00: ADC channel 00 INT3_0: External Interrupt 3_0 LED0: LED serial dot matrix COM0: Large current sink port PWM0_A1: PWM0_A1 Output port
7	7	Default function: Ground <VSS>
8	8	Default function: Power supply <VCC>
9	9	Default function: GPIO <PA1> other functions: SNS25: Touch key channel 25 ADC25: ADC channel 25 INT3_22: External Interrupt 3_22 SDA0_A: The serial data line of IIC TXD0_A: Serial port send TXD0_E: Serial port send SCL0_C: Serial clock line of IIC SWE0: Single-wire emulation port PGD0: Burning port
10	10	Default function: GPIO <PA0> other functions: SNS24: Touch key channel 24 ADC24: ADC channel 24 INT3_21: External Interrupt 3_21 RXD0_A: Serial port receiving TXD0_F: Serial port send SCL0_A: Serial clock line of IIC PGC0: Burning port
11	11	Default function: GPIO <PD7> other functions: SNS23: Touch key channel 23 ADC23: ADC channel 23 INT2: External Interrupt2 RXD0_F: Serial port receiving PGC2: Burning port

12	12	Default function: GPIO <PD6> other functions: SNS22: Touch key channel 22 ADC22: ADC channel 22 INT1: External Interrupt1 SDA0_C: The serial data line of IIC RXD0_E : Serial port receiving SWE2: Single-wire emulation port PGD2: Burning port
13	13	Default function: GPIO <PD5> other functions: SNS21: Touch key channel 21 ADC21: ADC channel 21 INT3_20: External Interrupt 3_20 TXD1_C: Serial port send PGC1: Burning port
14	14	Default function: GPIO <PD4> other functions: SNS20: Touch key channel 20 ADC20: ADC channel 20 INT3_19: External Interrupt 3_19 RXD1_C: Serial port receiving SWE1: Single-wire emulation port PGD1: Burning port
15	15	Default function: GPIO <PD3> other functions: SNS19: Touch key channel 19 ADC19: ADC channel 19 INT3_18: External Interrupt 3_18 XTAL_IN: External crystal input
16	16	Default function: GPIO <PD2> other functions: SNS18: Touch key channel 18 ADC18: ADC channel 18 INT3_17: External Interrupt 3_17 XTAL_OUT: External crystal output
17	-	Default function: GPIO <PD1> other functions: SNS17: Touch key channel 17 ADC17: ADC channel 17 INT3_16: External Interrupt 3_16 PWM1_B: PWM1_B Output port
18	17	Default function: GPIO <PD0> other functions: SNS16: Touch key channel 16 ADC16: ADC channel 16 INT0: External Interrupt 0 PWM1_A: PWM1_A Output port
19	-	Default function: GPIO <PC7>

		other functions: SNS15: Touch key channel 15 ADC15: ADC channel 15 INT3_15: External Interrupt 3_15 PWM0_A10: PWM0_A10 Output port
20	-	Default function: GPIO <PC6> other functions: SNS14: Touch key channel 14 ADC14: ADC channel 14 INT3_14: External Interrupt 3_14 PWM0_A9: PWM0_A9 Output port
21	-	Default function: GPIO <PC5> other functions: SNS13: Touch key channel 13 ADC13: ADC channel 13 INT3_13: External Interrupt 3_13 PWM0_A8: PWM0_A8Output port
22	-	Default function: GPIO <PC4> other functions: SNS12: Touch key channel 12 ADC12: ADC channel 12 INT3_12: External Interrupt 3_12
23	-	Default function: GPIO <PC3> other functions: SNS11: Touch key channel 11 ADC11: ADC channel 11 INT3_11: External Interrupt 3_11 PWM0_A7: PWM0_A7 Output port
24	-	Default function: GPIO <PC2> other functions: SNS10: Touch key channel 10 ADC10: ADC channel 10 INT3_10: External Interrupt 3_10
25	18	Default function: GPIO <PC1> other functions: SNS9: Touch key channel 9 ADC09: ADC channel 09 INT3_9: External Interrupt 3_9 TXD0_D: Serial port send
26	-	Default function: GPIO <PC0> other functions: SNS8: Touch key channel 8 ADC08: ADC channel 08 INT3_8: External Interrupt 3_8 PWM0_A6: PWM0_A6 Output port SDA0_B: The serial data line of IIC RXD0_D: Serial port receiving
27	19	Default function: GPIO <PB7> other functions: SNS7: Touch key channel 7 ADC07: ADC channel 07

		INT3_7: External Interrupt 3_7 LED7: LED serial dot matrix COM7: Large current sink port TXD1_B: Serial port send
28	20	Default function: GPIO <PB6> other functions: SNS6: Touch key channel 6 ADC06: ADC channel 06 INT3_6: External Interrupt 3_6 LED6: LED serial dot matrix COM6: Large current sink port RXD1_B: Serial port receiving

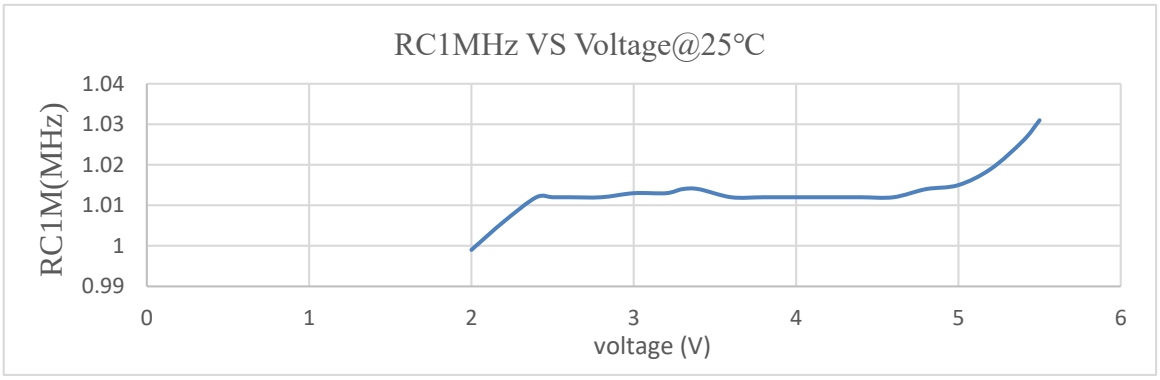
package pin correspondence diagram

2. Electrical Characteristics

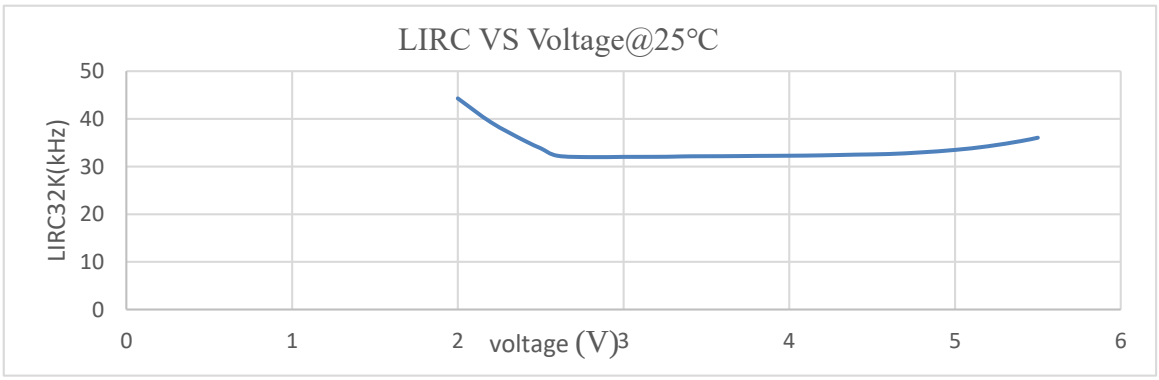
2.1. AC Characteristics

Parameter	Symbol	Conditions		Min	Typ	Max	Unit
		VCC	Temperature				
f_{RC1M}	Internal high-speed RC oscillator	5V	-20℃~65℃	-1%	1	+1%	MHz
			-40℃ ~105℃	-3%	1	+3%	
		2.7V~5.5V	25℃	-1%	1	+1%	
			-40℃ ~105℃	-3%	1	+3%	
f_{SYS}	System clock	5V	-20℃~65℃	-1%	12/6/4/1	+1%	MHz
			-40℃ ~105℃	-3%	12/6/4/1	+3%	
		2.7V~5.5V	25℃	-1%	12/6/4/1	+1%	
			-40℃ ~105℃	-3%	12/6/4/1	+3%	
f_{LIRC}	Internal low-speed RC oscillator	5V	25℃	-20%	32	+20%	kHz
			-40℃ ~105℃	-35%	32	+35%	
		2.7V~5.5V	25℃	-35%	32	+35%	

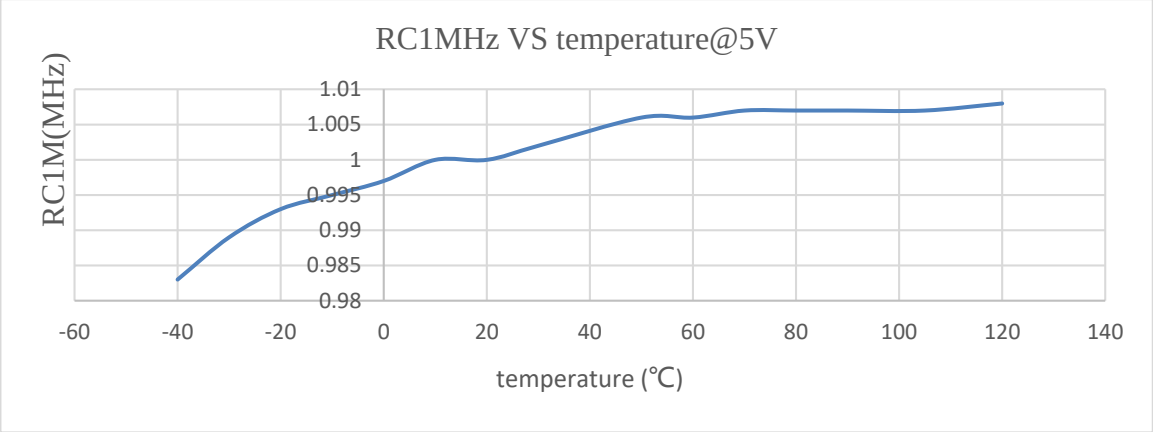
AC characteristics parameters table



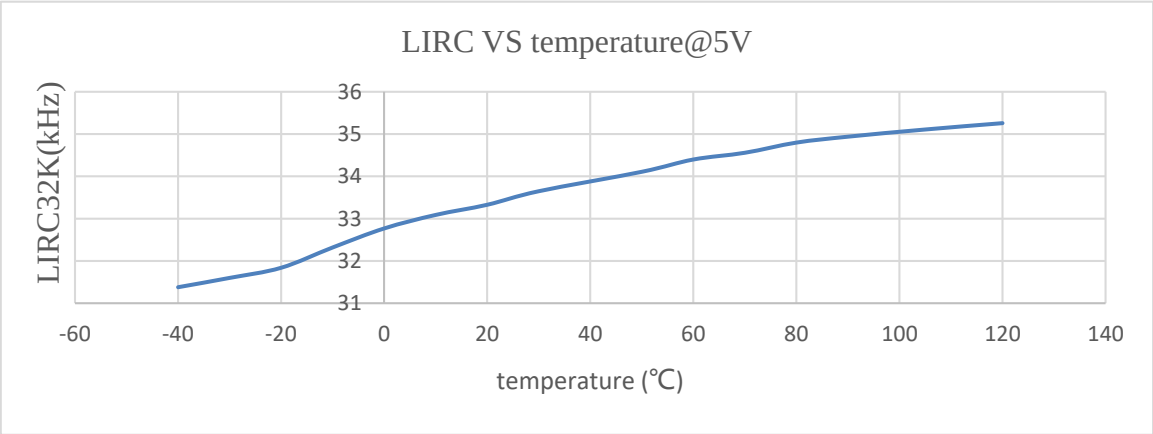
RC1M voltage curve



LIRC voltage curve



RC1M temperature curve



LIRC temperature curve

2.2. DC Characteristics

Ta=25℃

Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
		VCC	Conditions				
VCC	Operating voltage	-	-	2.7	-	5.5	V
I_{OP}	Active mode current	3.3V	f_{SYS}=12MHz, no load, all peripherals off	-	4.72	5.68	mA
		5V		-	4.74	5.68	
		3.3V	f_{SYS} =6MHz, no load, all peripherals off	-	2.96	3.55	
		5V		-	2.98	3.57	
		3.3V	f_{SYS} =4MHz, no load, all peripherals off	-	2.37	2.84	
		5V		-	2.39	2.86	
		3.3V	f_{SYS} =1MHz, no load, all peripherals off	-	1.50	1.80	
		5V		-	1.52	1.82	
I_{STB0}	idle mode 0 current	3.3V	f_{SYS} is off, no load, IO output low, all peripherals off	-	3.22	-	mA
		5V		-	3.25	-	
I_{STB1}	idle mode 1 current	3.3V	f_{RC1M} is off,, no load, IO output low, all peripherals off	-	11	-	μA
		5V		-	10	-	
I_{STB2}	Average current for intermittent wake-up from idle mode 1	3.3V	WDT_CTRL=7, WDT interrupt 2s wake up, 2ms working time, IO output is low, close other functions	-	14.7	-	μA
		5V		-	13.7	-	
		3.3V	Timer2 external crystal oscillator wakes up in 2s, 2ms working time, IO output is low, and other functions are closed	-	14.7	-	μA
		5V		-	13.7	-	
V_{IL}	Input low level	2.7~5.5V	-	-	-	0.3*VCC	V
V_{IH}	Input high level	2.7~5.5V	-	0.7*VCC	-	-	V
V_{INTL}	INT input low level	2.7~5.5V	-	-	-	0.3*VCC	V
V_{INTH}	INT input high level	2.7~5.5V	-	0.7*VCC	-	-	V
V_{OL}	output low voltage	5V	I_{OL}=50mA	-	-	0.1*VCC	V
V_{OH}	output high voltage	5V	I_{OH}=19mA	0.9*VCC	-	-	V

I_{OL}	IO sink current	5V	V_{OL}=0.1VCC	45	50	62	mA
I_{OH}	IO Source current	5V	V_{OH}=0.9VCC	17	19	24	mA
I_{COM}	PB large sink current	5V	V_{OL}=0.1VCC	-	110	-	mA
I_{Leak}	Input leakage current	5V	-	-	1	5	μA
R_{PH}	IO internal pull-up	5V	-	3.3	4.7	6.1	kΩ
R_{BPH}	PB pull-up	5V	-	21	30	39	kΩ
R_{BPH}	PB pull-down	5V	-	21	30	39	kΩ

The working current of the module is shown in the table below:

Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
		VCC	Conditions				
I_{BOR}	BOR operating current	5V	In idle mode 1, no load, BOR enabled		15.5	-	μA
I_{LVDT}	LVDT operating current	5V	In idle mode 1, no load, LVDT enabled, voltage selection 3.8V	-	15.5	-	μA
I_{CSD}	CSD operating current	5V	f_{SYS}=12MHz, no load, enable six channels of CSD and timer0, close other peripherals	-	1.2	-	mA
I_{ADC}	ADC operating current	5V	f_{SYS}=12MHz, no load, ADC enable, open a channel, GET_ADC scan, close other peripherals	-	0.9	-	mA
I_{PWM}	PWM operating current	5V	f_{SYS}=12MHz, no load, PWM0 is enabled, other peripherals are turned off	-	0.2	-	mA
I_{ERASE}	Page erase Current	5V	No load, enable DATA, only DATA is erased in while, and other peripherals are turned off	-	2.7	-	mA
I_{PROG}	Programming current	5V	No load, enable DATA, write only one byte in while, close other peripherals	-	3.2	-	mA

2.3. ADC Characteristics

Ta=25℃

Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
		VCC	Conditions				
V_{ADC}	Supply Voltage	-	-	2.7	-	5.5	V
N_R	Accuracy	-	-	-	9	10	Bit
V_{ADCI}	ADC Input voltage	-	-	VSS	-	V_{REF}	V
R_{ADCI}	ADC Input resistance	5V	No RC filtering	-	2.3	-	kΩ
			RC filtering	-	12	-	
I_{ADC}	ADC operating current	5V	f_{SYS}=12MHz, enable ADC, open a channel	-	0.9	-	mA
I_{ADCI}	input current	-	-	-	-	1	μA
DNL	Differential nonlinear error	5V	-	-	±4	±6	LSB
INL	Integral nonlinear error	5V	-	-	±4	±6	LSB
t2	ADC sampling time	-	-	1.3	-	-	μs
t_{ADC}	ADC conversion time	-	-	7.28	-	-	μs
RESO	Resolution	-	-	12			Bit
N_{ADC}	Input channel	-	-	-	-	26	Channel

ADC characteristic parameter table

2.4. Limit Parameters

Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
		VCC	Conditions				
VCC	Supply voltage when working	-	-	VSS+2.7	-	VSS+5.5	V
T_{STG}	Non-working storage temperature	-	-	-40	-	125	℃
Ta	Operating temperature	-	-	-40	-	105	℃
Vin	I/O input voltage	-	-	VSS-0.5	-	VCC+0.5	V
I_{OLA}	IOL total current	-	-	130			mA
I_{OHA}	IOH total current	-	-	-130			mA
ESD(HBM)	Port electrostatic discharge voltage	-	-	-2	-	2	kV

Limit parameters characteristics parameters table

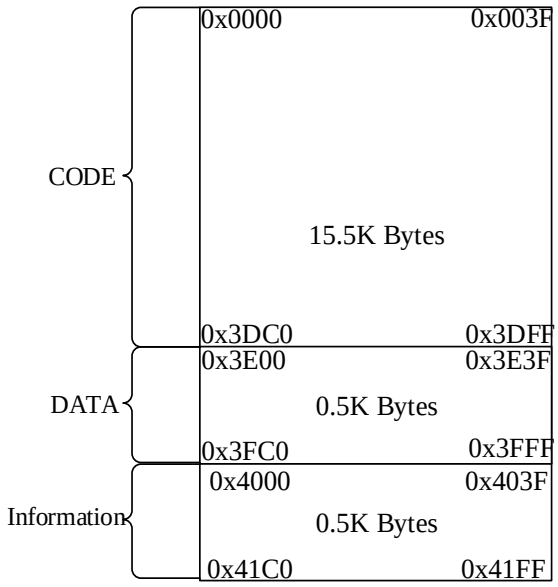
Notes: Exceed the limit parameters may cause damage to the chip, unable to expect the chip work outside the above indicated range. If you work under conditions outside the marked range for a long time, it may affect the reliability of the chip.

3. RAM, FLASH and SFR

3.1. Flash

FLASH memory features are as follows:

- CODE area: ICP programming supports block erase, page erase, byte write
- DATA area: support page erase, byte write
- Program/erase times: CODE area: at least 20000 times @25℃
  DATA area: at least 20000 times @25℃:
- Data retention period: 100 years@25℃
  10 years@85℃
- Support IAP online upgrade, 4K BOOT function area



Flash Storage Architecture

Module	Space size (Bytes)	Address	Page
CODE	15.5K	0x0000~0x3DFF	31
DATA	0.5K	0x3E00~0x3FFF	1
Information Block	0.5K	0x4000~0x41FF	1

Steps to read the unique identification code (UID) of the chip:

1. Turn off the interrupt;
2. Read CODE absolute address 0x41A8~0x41B7 corresponding to product ID1~ID16;
3. Restore the interrupt setting.

3.2. RAM

There are 256 Bytes internal, the address is 00H~FFH, including working registers group, bit addressing areas, buffers and SFR, the buffer contain the stack area.

Internal low 128 Bytes, 00H~7FH has 128 Bytes. Read and write data by immediate addressing or indirect addressing.

Internal high 128 Bytes, 80H~FFH has 128 Bytes. Read and write data only by immediate addressing or indirect addressing.

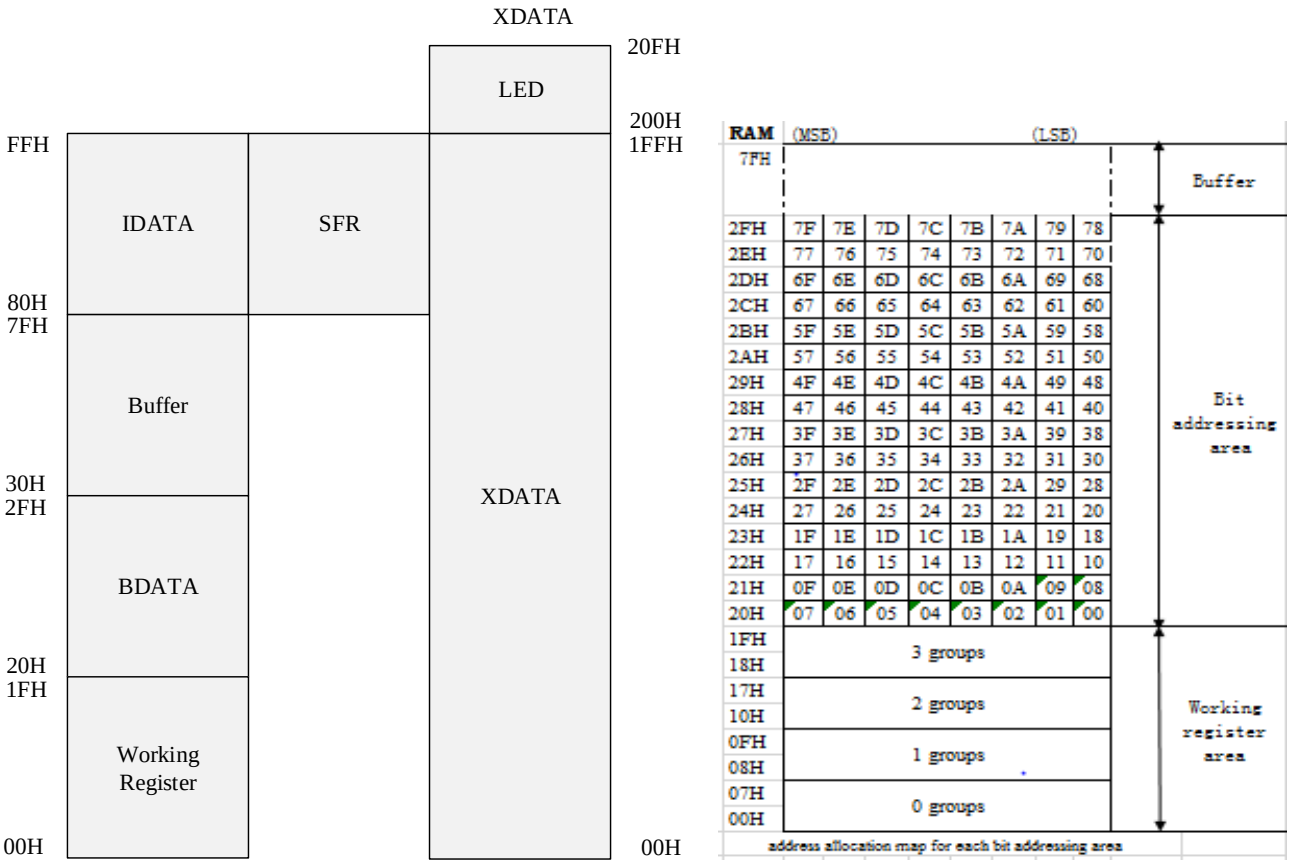
Special function register SFR: the address is 80H~FFH, Read and write data only by direct addressing.

Xdata has 1K Bytes, the address is 0000H~01FFH, users can use this area completely. To read and write data through the data pointer or working registers group addressing mode.

The LED storage RAM occupies the XRAM bus, the address is200~20FH.

Note reserved stack space when writing a program, in order to avoid stack overflow and program goes wrong. Stack first address automatically assigned by program, when programming with C language, but it must be stored in data or idata. KEIL stack can be set in the first address in STARTUP.A51.

RAM address space allocation map:



The following table lists the methods to get value in the three parts of RAM:

DATA	MOV A, direct
	MOV direct, A
	MOV direct, #data
	MOV direct1, direct2
	MOV Rn, direct
	MOV direct, Rn

IDATA	MOV A, @Ri
	MOV @Ri, A
	MOV direct, @Ri
	MOV @Ri, direct
	MOV @Ri, #data

XDATA	MOVX @DPTR, A MOVX A, @DPTR

RAM value instruction set

Notes: n: 0~7, i: 0~1.

3.3. SFR Table

Addr	Name	R/W	Reset value	Function description
0x80	DATAB	RW	1111_1111b	PB data register
0x81	SP	RW	0000_0111b	Stack pointer register
0x82	DPL	RW	0000_0000b	Data pointer register0 low 8-bit
0x83	DPH	RW	0000_0000b	Data pointer register0 high 8-bit
0x84	SYS_CLK_CFG	RW	xxxx_x001b	Clock control register
0x85	INT_PE_STAT	RW	xxxx_xx00b	WDT/Timer2 interrupt status register
0x86	INT_POBO_STAT	RW	xxxx_xx00b	LVDT boost/LVDT buck interrupt status register
0x87	PCON	RW	xxxx_xxx0b	Idle mode 1 select register
0x88	TCON	RW	0000_0x0xb	Timer control register
0x89	TMOD	RW	xx00_xx00b	Timer mode register
0x8A	TL0	RW	0000_0000b	Timer 0 counter low 8 bits
0x8B	TL1	RW	0000_0000b	Timer 1 counter low 8 bits
0x8C	TH0	RW	0000_0000b	Timer 0 counter high 8 bits
0x8D	TH1	RW	0000_0000b	Timer 1 counter high 8 bits
0x8E	SOFT_RST	RW	0000_0000b	Soft reset register
0x90	DATAC	RW	1111_1111b	PC port data register
0x91	WDT_CTRL	RW	xxxx_x000b	WDT timing overflow control register
0x92	WDT_EN	RW	0000_0000b	WDT timing enable register
0x93	TIMER2_CFG	RW	xxxx_x000b	TIMER2 CFG register
0x94	TIMER2_SET_H	RW	0000_0000b	TIMER2 count value configuration register, high 8 bits
0x95	TIMER2_SET_L	RW	0000_0000b	TIMER2 count value configuration register, low 8 bits
0x96	REG_ADDR	RW	xx00_0000b	Second address bus register
0x97	REG_DATA	RW	0000_0000b	Second data read and write bus register
0x98	DATAD	RW	1111_1111b	PD port data register
0x99	PWM0_L_L	RW	xxxx_0000b	PWM0 low level control register (low 4 bits)
0x9A	PWM0_L_H	RW	0000_0000b	PWM0 low level control register (high 8 bits)
0x9B	PWM0_H_L	RW	xxxx_0000b	PWM0 high level control register (low 4 bits)
0x9C	PWM0_H_H	RW	0000_0000b	PWM0 high level control register (high 8 bits)
0x9D	PWM1_L_L	RW	xxxx_0000b	PWM1 low level control register (low 4 bits)
0x9E	PWM1_L_H	RW	0000_0000b	PWM1 low level control register (high 8 bits)
0x9F	PWM1_H_L	RW	xxxx_0000b	PWM1 high level control register (low 4 bits)
0xA0	P2_XH	RW	1111_1111b	MOVX @Ri,A operation xdata address high 8 bits
0xA1	PWM1_H_H	RW	0000_0000b	PWM1 high level control register (high 8 bits)

0xA2	PWM_CTRL	RW	xx00_0000b	PWM control register
0xA3	PWM_CLK_SEL	RW	xx00_0000b	PWM clock prescaler selection register
0xA4	OSC_SFR_SEL	RW	xxxx_xx00b	ADJ_OSC selection register
0xA5	ADJ_OSC_H	RW	1111_1111b	Configuration word register
0xA6	ADJ_OSC_L	RW	xxxx_xx11b	Configuration word register
0xA8	IEN0	RW	0xxx_0000b	Interrupt enable register
0xAA	SEL_SEN_SR_I	RW	xxxx_0000b	CSD slope control register
0xAB	LED_IO_START	RW	xxxx_0000b	LED port matrix start PAD selection register
0xAC	PERIPH_IO_SEL3	RW	x000_0000b	INT3 select enable register 3
0xAD	PERIPH_IO_SEL2	RW	0000_0000b	INT3 select enable register 2
0xAE	PERIPH_IO_SEL1	RW	0000_0000b	INT3 select enable register 1
0xAF	SCAN_START	RW	xxxx_xxx0b	LED scan-opening register
0xB0	DP_CON	RW	xxx0_0000b	LED scan control register
0xB1	SCAN_WIDTH	RW	0000_0000b	LED scan on time 1 control register
0xB2	LED2_WIDTH	RW	0000_0000b	LED scan on time 2 control register
0xB3	LED_DRIVE	RW	xxxx_0000b	LED drive capability configuration register
0xB4	ADC_SPT	RW	0000_0000b	ADC sample time configure register
0xB5	ADC_SCAN_CFG	RW	xx00_0000b	ADC scan control register
0xB6	ADCCKC	RW	xxxx_0000b	ADC clock control register
0xB8	IPL0	RW	xxxx_0000b	Interrupt priority register 0
0xB9	ADC_RDATAH	R	xxxx_0000b	ADC scan result register, high 4 bits
0xBA	ADC_RDATAL	R	0000_0000b	ADC scan result register, low 8 bits
0xBB	ADC_CFG1	RW	0000_0000b	ADC sampling timing control register 1
0xBC	ADC_CFG2	RW	xx00_0111b	ADC sampling timing control register 2
0xBD	UART0_BDL	RW	0000_0000b	UART0 baud rate control register
0xBE	UART0_CON1	RW	0000_0000b	UART0 control register 1
0xBF	UART0_CON2	RW	xxx0_1100b	UART0 control register 2
0xC0	UART0_STATE	R/RW	x000_0000b	UART0 status flag register
0xC1	UART0_BUF	RW	1111_1111b	UART0 data flag register
0xC2	COM_IO_SEL	RW	0000_0000b	COM selection configuration register
0xC3	ODRAIN_EN	RW	xxxx_x000b	PA0/PA1/PD6 port open drain output enable register
0xC4	BOR_SEL	RW	xxxx_1000b①	BOR control register
0xC5	UART1_BDL	RW	0000_0000b	UART1 baud rate control register
0xC6	UART1_CON1	RW	0000_0000b	UART1 control register 1
0xC7	UART1_CON2	RW	xxx0_1100b	UART1 control register 2
0xC8	UART1_STATE	R/RW	x000_0000b	UART1 status flag register
0xC9	UART1_BUF	RW	1111_1111b	UART1 data register
0xCA	CSD_START	RW	xxxx_xxx0b	CSD scan open register

0xCB	SNS_SCAN_CFG1	RW	x000_0000b	Touch key scan configuration register 1
0xCC	SNS_SCAN_CFG2	RW	x100_0000b	Touch key scan configuration register 2
0xCD	SNS_SCAN_CFG3	RW	x111_0000b	Touch key scan configuration register 3
0xCE	CSD_RAWDATAL	R	0000_0000b	CSD counter, low 8-bit
0xCF	CSD_RAWDATAH	R	0000_0000b	CSD counter, high 8-bit
0xD0	PSW	R/RW	0000_0000b	Program status word register
0xD1	PULL_I_SELA_L	RW	0000_0000b	CSD pull-up current source selection register
0xD2	SNS_ANA_CFG	RW	xx10_1101b	CSD scan parameter configuration register
0xD3	SNS_IO_SEL1	RW	0000_0000b	SNS channel select register 1
0xD4	SNS_IO_SEL2	RW	0000_0000b	SNS channel select register 2
0xD5	SNS_IO_SEL3	RW	0000_0000b	SNS channel select register 3
0xD6	SNS_IO_SEL4	RW	xxxx_xx00b	SNS channel select register 4
0xD7	RST_STAT	RW	0000_0010b②	Reset flag register
0xD8	PD_PB	RW	0000_0000b	PB port pull-down resistor control register
0xD9	ADC_IO_SEL1	RW	0000_0000b	ADC function selection register 1
0xDA	ADC_IO_SEL2	RW	0000_0000b	ADC function selection register 2
0xDB	ADC_IO_SEL3	RW	0000_0000b	ADC function selection register 3
0xDC	ADC_IO_SEL4	RW	xxxx_xx00b	ADC function selection register 4
0xDD	PU_PA	RW	xxxx_xx00b	PA port pull-up resistor control register
0xDE	PU_PB	RW	0000_0000b	PB port pull-up resistor control register
0xDF	PU_PC	RW	0000_0000b	PC port pull-up resistor control register
0xE0	ACC	RW	0000_0000b	Accumulator
0xE1	IRCON2	RW	xxxx_0000b	Interrupt flag register 2
0xE2	PU_PD	RW	0000_0000b	PD port pull-up resistor control register
0xE3	IICADD	RW	0000_000xb	IIC address register
0xE4	IICBUF	RW	0000_0000b	IIC transmit and receive data register
0xE5	IICCON	RW	xx01_0000b	IIC configuration register
0xE6	IEN1	RW	0000_00xxb	Interrupt enable register 1
0xE7	IEN2	RW	xxxx_0000b	Interrupt enable register 2
0xE8	IICSTAT	R/RW	0100_0100b	IIC status register
0xE9	IICBUFFER	RW	0000_0000b	IIC transmit and receive data buffer register
0xEA	TRISA	RW	xxxx_xx11b	PA port direction register
0xEB	TRISB	RW	1111_1111b	PB port direction register
0xEC	TRISC	RW	1111_1111b	PC port direction register
0xED	TRISD	RW	1111_1111b	PD port direction register
0xEE	UART_IO_SEL	RW	xxx0_0000b	UART select enable register
0xEF	PWM0_IO_SEL	RW	xxxx_0000b	PWM0 select IO port configuration register
0xF0	B	RW	0000_0000b	B register
0xF1	IRCON1	RW	0000_00xxb	Interrupt flag register 1

0xF2	PERIPH_IO_SEL	RW	x100_0000b	IIC /INT function control register
0xF4	IPL2	RW	xxxx_0000b	Interrupt priority register 2
0xF6	IPL1	RW	0000_00xxb	Interrupt priority register 1
0xF7	EXT_INT_CON	RW	x001_0101b	External interrupt polarity control register
0xF8	DATAA	RW	xxxx_xx11b	PA data register
0xF9	SPROG_ADDR_H	RW	xx00_0000b	Address control register
0xFA	SPROG_ADDR_L	RW	0000_0000b	Address control register lower 8 bits
0xFB	SPROG_DATA	RW	0000_0000b	Data register
0xFC	SPROG_CMD	RW	0000_0000b	Command register
0xFD	SPROG_TIM	RW	xxx0_1010b	Erase and write time control register
0xFE	PD_ANA	RW	xx00_0111b	Module switch control register
0xFF	LVDT_SEL	RW	xxxx_1000b	LVDT control register

SFR register summary

Note:

1. **Registers whose addresses end with 8 or 0 can be bit-operated, such as register addresses 0x80 and 0x88.**
2. **R: read only; RW: read and write;**
3. **'x': Unsteady state;**
4. **'①': The reset value is the default value after power-on reset, and the value after the global reset is completed is the factory calibration value (WDT overflow reset, power on reset, brown-out reset, program reset, debug reset, PC pointer overflow reset, software reset, IAP operation BOOT upgrade reset);**
5. **'②': Power-on reset RST_STAT register reset value 0x02; other mode reset: the corresponding reset flag bit of RST_STAT register is 1, and other reset flag bits keep their original state.**

3.4. Secondary Bus Register Table

The BF7812AMXX-XJLX series supports expanded secondary bus registers for expanding more register functions. You only need to write the address of the secondary bus register to be accessed into REG_ADDR, and then access the corresponding secondary bus register through the REG_DATA register. It is recommended that when reading and writing secondary bus registers, first EA = 0, and then EA = 1 after the operation is completed. Prevent other interrupts or operations from modifying the address or data of the secondary bus register.

Addr	Name	Bit	R/W	Reset value	Function description
0x96	REG_ADDR	<5:0>	RW	0x00	Secondary bus address configuration register
0x97	REG_DATA	<7:0>	RW	0x00	Secondary bus data read and write register

Addr	Name	R/W	Reset value	Function description
0x01	CFG1_REG	R	1000_0110b①	Configuration word register 1
0x02	CFG2_REG	R	0111_1111b①	Configuration word register 2
0x03	CFG3_REG	R	1111_1111b①	Configuration word register 3
0x04	CFG4_REG	R	0011_0000b①	Configuration word register 4
0x05	CFG5_REG	R	0000_1111b①	Configuration word register 5
0x06	CFG6_REG	R	0001_1111b①	Configuration word register 6
0x07	CFG7_REG	R	0001_1111b①	Configuration word register 7
0x08	CFG8_REG	R	0111_1111b①	Configuration word register 8
0x09	CFG9_REG	R	0011_1111b①	Configuration word register 9
0x0A	CFG30_REG	R	1111_1111b①	Configuration word register30
0x21	FLASH_BOOT_EN	R	xxxx_xxx0b	BOOT mode status register
0x22	BOOT_CMD	RW	0000_0000b	Program space jump instruction register
0x23	ROM_OFFSET_L	R	0000_0000b	Address offset of CODE area (low 8 bits)
0x24	ROM_OFFSET_H	R	0000_0000b	Address offset of CODE area (high 8 bits)

Note:

1. '①': The reset value is the default value after power-on reset, and the value after the global reset is completed is the factory calibration value;
2. 'x': Unsteady state;
3. R: read only, RW: read and write.

4. Register Summary

4.1. SFR Register Detailed Description

DATAB (80H) PB port data register

Bit number	7	6	5	4	3	2	1	0
Symbol	PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	1	1	1	1	1	1	1	1

Bit number	Bit symbol	Description
7~0	--	The output level of the PB group can be configured as the GPIO port. The read value is the level state of the current IO port or the configured output value.

SP (81H) Stack pointer register

Bit number	7	6	5	4	3	2	1	0
Symbol	SP[7:0]							
R/W	R/W							
Reset value	7							

DPL(82H) Data pointer register0 low 8-bit

Bit number	7	6	5	4	3	2	1	0
Symbol	DPL[7:0]							
R/W	R/W							
Reset value	0							

DPH (83H) Data pointer register0 high 8-bit

Bit number	7	6	5	4	3	2	1	0
Symbol	DPH[7:0]							
R/W	R/W							
Reset value	0							

SYS_CLK_CFG (84H) Clock control register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	IM0_EN	PLL_CLK_SEL	
R/W	-	-	-	-	-	R/W	R/W	
Reset value	-	-	-	-	-	0	0	1

Bit number	Bit symbol	Description
7~3	--	Reserved
2	IM0_EN	Idle mode 0 enable 1: The chip enters Idle mode 0; 0: The chip exits Idle mode 0
1~0	PLL_CLK_SEL	PLL clock divided selection register 00: 12MHz; 01: 6MHz; 10: 4MHz; 11: 1MHz

INT_PE_STAT(85H)WDT/Timer2 interrupt status register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	-	INT_WDT_STAT	INT_TIMER2_STAT
R/W	-	-	-	-	-	-	R/W	R/W
Reset value	-	-	-	-	-	-	0	0

Bit number	Bit symbol	Description
1	INT_WDT_STAT	WDT interrupt status, set 0, write WDT_CTRL can set 0. 1: interrupt effective 0: invalid interrupt
0	INT_TIMER2_STAT	TIMER2 interrupt status, set 0, write TIMER2_CFG can set 0. 1: interrupt effective 0: invalid interrupt

INT_POBO_STAT (86H) LVDT boost/LVDT buck interrupt status register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	-	INT_PO_STAT	INT_BO_STAT
R/W	-	-	-	-	-	-	R/W	R/W
Reset value	-	-	-	-	-	-	0	0

Bit number	Bit symbol	Description
1	INT_PO_STAT	Lvdt boost interrupt status 1: boost interrupt is valid 0: boost interrupt is invaild
0	INT_BO_STAT	Lvdt buck interrupt state 1: buck interrupt is valid 0: buck interrupt is invalid

PCON(87H) Idle mode 1 select register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	-		IM1_EN
R/W	-	-	-	-	-	-	-	R/W
Reset value	-	-	-	-	-	-	-	0

Bit number	Bit symbol	Description
0	IM1_EN	Idle mode 1 control 1: Idle mode 1; 0: Normal mode, automatically cleared after wake-up Note: The software delay must be greater than or equal to 100 μs after wake-up, otherwise the wake-up function is abnormal

TCON(88H) Timer control register

Bit number	7	6	5	4	3	2	1	0
Symbol	TF1	TR1	TF0	TR0	IE1	-	IE0	-
R/W	R/W	R/W	R/W	R/W	R/W	-	R/W	-
Reset value	0	0	0	0	0	-	0	-

Bit number	Bit symbol	Description
7	TF1	Timer1 overflow flag. Set to 1 when Timer1 overflows, or Timer0's TH0 overflows in mode three.
6	TR1	Timer1 start enable.When set to 1, enable the Timer1 count or Timer0 TH0 count in mode 3.
5	TF0	Timer0 overflow flag. The hardware set 1 when Timer0 overflows.
4	TR0	Timer0 start enable, when set to 1, start Timer0 count.
3	IE1	External interrupt 1. The hardware set 1, the software is cleared.
1	IE0	External interrupt 0. The hardware set 1, the software is cleared
2, 0	--	Reserved

TMOD(89H) Timer mode register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	M1[1:0]		-	-	M0[1:0]	
R/W	-	-	R/W		-	-	R/W	
Reset value	-	-	0	0	-	-	0	0

Bit number	Bit symbol	Description
7~6, 3~2	--	Reserved
5~4	M1[1:0]	Timer1 mode select bits 00=mode0 – 13 bit timer 01=mode1 – 16 bit timer 10=mode2 – automatic reload mode 8bit timer 11=mode3 – 2*8bit timer

1~0	M0[1:0]	Timer0 mode select bits 00=mode0 – 13 bit timer 01=mode1 – 16 bit timer 10=mode2 – automatic reload mode 8bit timer 11=mode3 – 2*8bit timer

TL0(8AH) Timer 0 counter 8 bits

Bit number	7	6	5	4	3	2	1	0
Symbol	TL0[7:0]							
R/W	R/W							
Reset value	0							

TL1(8BH) Timer 1 counter low 8 bits

Bit number	7	6	5	4	3	2	1	0
Symbol	TL1[7:0]							
R/W	R/W							
Reset value	0							

TH0(8CH) Timer 0 counter high 8 bits

Bit number	7	6	5	4	3	2	1	0
Symbol	TH0[7:0]							
R/W	R/W							
Reset value	0							

TH1(8DH) Timer 1 counter high 8 bits

Bit number	7	6	5	4	3	2	1	0
Symbol	TH1[7:0]							
R/W	R/W							
Reset value	0							

SOFT_RST(8EH) Soft reset register

Bit number	7	6	5	4	3	2	1	0
Symbol	-							
R/W	R/W							
Reset value	0							

Bit number	Bit symbol	Description
7~0	--	Software reset register. Software reset is only generated when the register value is 0x55.

DATAC(90H) PC port data register

Bit number	7	6	5	4	3	2	1	0
Symbol	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	1	1	1	1	1	1	1	1

Bit number	Bit symbol	Description
7~0	--	PC data register. The output level of the PC group can be configured as the GPIO port. The read value is the level state of the current IO port or the configured output value.

WDT_CTRL(91H) WDT timing overflow control register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	WDT_TIME_SEL		
R/W	-	-	-	-	-	R/W		
Reset value	-	-	-	-	-	0	0	0

Bit number	Bit symbol	Description
7~0	WDT_TIME_SEL	WDT overflow timer register. Timing length is as follows: 0x00: 18ms; 0x01: 36ms; 0x02: 72ms; 0x03: 144ms; 0x04: 288ms; 0x05: 576ms; 0x06: 1152ms; 0x07: 2304ms;

WDT_EN(92H) WDT timing enable register

Bit number	7	6	5	4	3	2	1	0
Symbol	WDT_EN							
R/W	R/W							
Reset value	0							

Bit number	Bit symbol	Description
7~0	WDT_EN	WDT timing enable configuration register. WDT is turned off when the configuration value is 0x55.

TIMER2_CFG (93H) TIMER2 CFG register

Bit number	7~3	2	1	0
Symbol	-	TIMER2_CLK_SEL	TIMER2_RLD	TIMER2_EN
R/W	-	R/W	R/W	R/W
Reset value	-	0	0	0

Bit number	Bit symbol	Description
3	--	Reserved
2	TIMER2_CLK_SEL	TIMER2 clock select register 1: select XTAL32768Hz 0: select LIRC
1	TIMER2_RLD	TIMER2 reload enable control register 1: automatic reload mode 0: manual reload mode
0	TIMER2_EN	TIMER2 count enable register

		1: turn on timing; 0: stop timing; In manual reload mode, the hardware automatically clears this register after timing is completed, stop count. In manual reload mode, will maintain the enable register after the count is completed. Automatically re-counting from 0, no matter which mode, configuring this register to 1 during counting will start counting from 0.

TIMER2_SET_H(94H) TIMER2 count value configuration register, high 8 bits

Bit number	7	6	5	4	3	2	1	0
Symbol	-							
R/W	R/W							
Reset value	0							

Bit number	Bit symbol	Description
7~0	--	TIMER2 count configuration register, high 8 bits. Configuring this register during the scan will recount.

TIMER2_SET_L(95H) TIMER2 count value configuration register, low 8 bits

Bit number	7	6	5	4	3	2	1	0
Symbol	-							
R/W	R/W							
Reset value	0							

Bit number	Bit symbol	Description
7~0	--	TIMER2 count configuration register, low 8 bits. Configuring this register during the scan will recount.

DATAD(98H) PD port data register

Bit number	7	6	5	4	3	2	1	0
Symbol	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	1	1	1	1	1	1	1	1

Bit number	Bit symbol	Description
7~0	--	PD data register. The output level of the PD group can be configured as the GPIO port. The read value is the level state of the current IO port or the configured output value.

PWM0_L_L (99H) PWM0 low level control register (low 4 bits)

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	PWM0_L_L[3:0]			

R/W	-	-	-	-	R/W
Reset value	-	-	-	-	0

PWM0_L_H (9AH) PWM0 low level control register (high 8 bits)

Bit number	7	6	5	4	3	2	1	0
Symbol	PWM0_L_H[7:0]							
R/W	R/W							
Reset value	0							

PWM0_H_L (9BH) PWM0 high level control register (low 4 bits)

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	PWM0_H_L[3:0]			
R/W	-	-	-	-	R/W			
Reset value	-	-	-	-	0			

PWM0_H_H (9CH) PWM0 high level control register (high 8 bits)

Bit number	7	6	5	4	3	2	1	0
Symbol	PWM0_H_H[7:0]							
R/W	R/W							
Reset value	0							

PWM1_L_L (9DH) PWM1 low level control register (low 4 bits)

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	PWM1_L_L[3:0]			
R/W	-	-	-	-	R/W			
Reset value	-	-	-	-	0			

PWM1_L_H (9EH) PWM1 low level control register (high 8 bits)

Bit number	7	6	5	4	3	2	1	0
Symbol	PWM1_L_H[7:0]							
R/W	R/W							
Reset value	0							

PWM1_H_L (9FH) PWM1 high level control register (low 4 bits)

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	PWM1_H_L[3:0]			
R/W	-	-	-	-	R/W			
Reset value	-	-	-	-	0			

P2_XH (A0H) MOVX @Ri,A operation xdata address high 8 bits

Bit number	7	6	5	4	3	2	1	0
Symbol	P2_XH[7:0]							
R/W	R/W							
Reset value	FF							

Bit number	Bit symbol	Description

7~0	P2_XH[7:0]	When using the MOVX @Ri, A instruction, when operating the pdata area, P2_XH need to be clear to 0.

PWM1_H_H (A1H) PWM1 high level control register (high 8 bits)

Bit number	7	6	5	4	3	2	1	0
Symbol	PWM1_H_H[7:0]							
R/W	R/W							
Reset value	0							

PWM_EN (A2H) PWM control register

Bit number	7	6	5	4
Symbol	-	-	PWM1_CH1_ POLA_SEL	PWM1_CH0_ POLA_SEL
R/W	-	-	R/W	R/W
Reset value	-	-	0	0
Bit number	3	2	1	0
Symbol	PWM1_CH1_EN	PWM1_CH0_EN	PWM1_EN	PWM0_EN
R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0

Bit number	Bit symbol	Description
7~6	--	Reserved
5	PWM1_CH1_ POLA_SEL	PWM1_B channel polarity selection 1: The count value overflows, making the output low; 0: The count value overflows, making the output high
4	PWM1_CH0_ POLA_SEL	PWM1_A channel polarity selection 1: The count value overflows, making the output low; 0: The count value overflows, making the output high
3	PWM1_CH1_EN	PWM1_B channel enable 1: enable; 0: Disable
2	PWM1_CH0_EN	PWM1_A channel enable 1: enable; 0: disable
1	PWM1_EN	PWM1 module enable register 1: enable; 0: disable
0	PWM0_EN	PWM0 module enable register 1: enable; 0: disable

PWM_CLK_SEL(A3H) PWM clock prescaler selection register

Bit number	7	6	5	4	3	2	1	0

Symbol	-	-	PWM1_CLK_SEL			PWM0_CLK_SEL		
R/W	-	-	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	-	-	0	0	0	0	0	0

Bit number	Bit symbol	Description
7~6	--	Reserved
5~3	PWM1_CLK_SEL	PWM1 clock prescaler selection register 000: Divided by 1---24MHz 001: Divided by 2---12MHz 010: Divided by 4---6MHz 011: Divided by 6---4MHz 100: Divided by 8---3MHz 101: Divided by 12---2MHz 110: Divided by 14---1.7MHz 111: Divided by 16---1.5MHz
2~0	PWM0_CLK_SEL	PWM0 clock prescaler selection register 000: Divided by 1---24MHz 001: Divided by 2---12MHz 010: Divided by 4---6MHz 011: Divided by 6---4MHz 100: Divided by 8---3MHz 101: Divided by 12---2MHz 110: Divided by 14---1.7MHz 111: Divided by 16---1.5MHz

OSC_SFR_SEL(A4H) ADJ_OSC selection register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	-	-	-
R/W	-	-	-	-	-	-	R/W	R/W
Reset value	-	-	-	-	-	-	0	0

Bit number	Bit symbol	Description
1~0	--	Register ADJ_OSC effective value selection 10: Select SFR write value; Other: select configuration word Note: Read the OSC calibration value and control it within ±10% of { CFG3_REG[7:0], CFG2_REG[1:0]} calibration value

ADJ_OSC_H(A5H) Configuration word register

Bit number	7	6	5	4	3	2	1	0
Symbol	ADJ_OSC[9:2]							

R/W	R/W
Reset value	FF

Bit number	Bit symbol	Description
7~0	ADJ_OSC[9:2]	Configuration word register The written value is SFR, the read value is the effective value, and the configuration word or SFR is selected according to OSC_SFR_SEL

ADJ_OSC_L(A6H) Configuration word register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	-	ADJ_OSC[1:0]	
R/W	-	-	-	-	-	-	R/W	R/W
Reset value	-	-	-	-	-	-	1	1

Bit number	Bit symbol	Description
1~0	ADJ_OSC[1:0]	Configuration word register The written value is SFR, the read value is the effective value, and the configuration word or SFR is selected according to OSC_SFR_SEL

IEN0(A8H) Interrupt enable register

Bit number	7	6	5	4	3	2	1	0
Symbol	EA	-	-	-	ET1	EX1	ET0	EX0
R/W	R/W	-	-	-	R/W	R/W	R/W	R/W
Reset value	0	-	-	-	0	0	0	0

Bit number	Bit symbol	Description
7	EA	Interrupt enable bit 0: Mask all interrupts (EA has priority over the respective interrupt enable bits of the interrupt sources); 1: The interrupt is turned on. Whether the interrupt request of each interrupt source is allowed or forbidden is determined by the respective enable bit.
6~4	--	Reserved
3	ET1	Timer1 interrupt enable bit 0: Disable timer 1 to apply for interrupt; 1: Allow timer 1 flag bit to apply for interrupt.
2	EX1	INT_EXT1 enable bit 0: Disable INT_EXT1 to apply for interrupt; 1: Allow INT_EXT1 to apply for interrupt.
1	ET0	Timer 0 interrupt enable bit

		0: Disable timer 0 (TF0) to apply for interrupt; 1: Allow TF0 flag bit to request interrupt.
0	EX0	INT_EXT0 enable bit 0: Disable INT_EXT0 to apply for interrupt; 1: Allow INT_EXT0 to apply for interrupt.

SEL_SEN_SR_I(AAH) CSD slope control register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	-	-	-
R/W	-	-	-	-	R/W	R/W	R/W	R/W
Reset value	-	-	-	-	0	0	0	0

Bit number	Bit symbol	Description
3~0	--	CSD slope control register 1111: Fast slope Other: reserved

LED_IO_START(ABH) LED port matrix start PAD selection register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	-	-	-
R/W	-	-	-	-	R/W	R/W	R/W	R/W
Reset value	-	-	-	-	0	0	0	0

Bit number	Bit symbol	Description
3~0	--	LED port matrix start PAD selection register 0000: PB0 port; 0001: PB1 port; 0010: PB2 port; 0011: PB3 port; 0100: PB4 port; 0101: PB5 port; 0110: PB6 port; 0111: PB7 port; 1000: PC0 port; Other: PB0 port The starting port LED0 selects the specific position of the PAD, and the remaining LEDX are arranged in order from top to bottom, and if PC0 is exceeded, they are arranged in cyclic order from PB0. For example: LED_IO_START=0111, DUTY_SEL=7, then LED0: PB7, LED1: PC0, LED2: PB0, LED3: PB1, LED4: PB2, LED5: PB3, LED6: PB4, LED7: PB5, LED8: PB6

PERIPH_IO_SEL3(ACH) INT3 select enable register 3

Bit number	7	6	5	4
Symbol	-	INT3_22_IO_SEL	INT3_21_IO_SEL	INT3_20_IO_SEL
R/W	-	R/W	R/W	R/W
Reset value	-	0	0	0
Bit number	3	2	1	0

Symbol	INT3_19_IO_SEL	INT3_18_IO_SEL	INT3_17_IO_SEL	INT3_16_IO_SEL
R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0

Bit number	Bit symbol	Description
6~0	INT3_n_IO_SEL (n=22~16)	INT3_n port selection enable 1: Select INT function; 0: INT function is not selected

PERIPH_IO_SEL2(ADH) INT3 select enable register 2

Bit number	7	6	5	4
Symbol	INT3_15_IO_SEL	INT3_14_IO_SEL	INT3_13_IO_SEL	INT3_12_IO_SEL
R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0
Bit number	3	2	1	0
Symbol	INT3_11_IO_SEL	INT3_10_IO_SEL	INT3_9_IO_SEL	INT3_8_IO_SEL
R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0

Bit number	Bit symbol	Description
7~0	INT3_n_IO_SEL (n=15~8)	INT3_n port selection enable 1: Select INT function; 0: INT function is not selected

PERIPH_IO_SEL1(AEH) INT3 select enable register 1

Bit number	7	6	5	4
Symbol	INT3_7_IO_SEL	INT3_6_IO_SEL	INT3_5_IO_SEL	INT3_4_IO_SEL
R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0
Bit number	3	2	1	0
Symbol	INT3_3_IO_SEL	INT3_IO_2_SEL	INT3_1_IO_SEL	INT3_0_IO_SEL
R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0

Bit number	Bit symbol	Description
7~0	INT3_n_IO_SEL (n=7~0)	INT3_n port selection enable 1: Select INT function; 0: INT function is not selected

SCAN_START(AFH) LED scan open register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	-	-	-

R/W	-	-	-	-	-	-	-	R/W
Reset value	-	-	-	-	-	-	-	0

Bit number	Bit symbol	Description
0	--	LED scan on register 1: Scan on; 0: Scan off

DP_CON (B0H) LED scan control register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	DUTY_SEL			SCAN_MODE	COM_MOD
R/W	-	-	-	R/W			R/W	R/W
Reset value	-	-	-	0	0	0	0	0

Bit number	Bit symbol	Description
4~2	DUTY_SEL	LED port drive mode matrix selection configuration register 0: no matrix; 1: 4x4 matrix; 2: 4x5 matrix; 3: 5x6 matrix; 4: 6x7 matrix; 5: 7x7 matrix; 6: 7x8 matrix; 7: 8x8 matrix
1	SCAN_MODE	LED scan mode. 1: cycle scan mode 0: interrupt scan mode
0	COM_MOD	Large sink current ports drive enable. 1: COM port function lock, work as a large current IO port. 0: COM port function is not locked and can be configured as other functions. When the COM port locks the large sink current IO port, by configuring GPIO registers output drive timing, it is vaild when all of the following LED scan configurations are invalid.

SCAN_WIDTH (B1H) LED scan on time 1 control register

Bit number	7	6	5	4	3	2	1	0
Symbol	-							
R/W	R/W							
Reset value	0							

Bit number	Bit symbol	Description
7~0	--	In the LED dot matrix drive mode, the corresponding single lamp lighting time configuration register-the first segment of lamp cycle configuration period=(scan_width+1)*16us, support configuration range 0.016~4.096ms

LED2_WIDTH (B2H) LED scan on time 2 control register

Bit number	7	6	5	4	3	2	1	0
Symbol	-							
R/W	R/W							
Reset value	0							

Bit number	Bit symbol	Description
7~0	--	In the LED dot matrix drive mode, the corresponding single lamp lighting time configuration register-the second stage of lamp cycle configuration period=(led2_width+1)*16us, support configuration range 0.016~4.096ms

LED2_DRIVE (B3H) LED drive capability configuration register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-			
R/W	-	-	-	-	R/W			
Reset value	-	-	-	-	0			

Bit number	Bit symbol	Description
3~0	-	LED port drive capability configuration register 0~15------4mA~72mA, please refer to LED drive ammeter for details.

ADC_SPT (B4H) ADC sample time configure register

Bit number	7	6	5	4	3	2	1	0
Symbol	ADC_SPT							
R/W	R/W							
Reset value	0							

Bit number	Bit symbol	Description
7~0	ADC_SPT	ADC sample time configure register sample time: t2 = 4 * (ADC_SPT+1) * t_{ADCK}

ADC_SCAN_CFG (B5H) ADC scan control register

Bit number	7	6	5	4	3	2	1	0

Symbol	-	-	ADC_ADDR	ADC_START
R/W	-	-	R/W	R/W
Reset value	-	-	0	0

Bit number	Bit symbol	Description
5~1	ADC_ADDR	ADC channel address selection register 00000: corresponds to ADC0; 00001: corresponding to ADC1; ... 11000: corresponding to ADC24; 11001: corresponding to ADC25; 11010: corresponding to ADC26_VREF; other: reserved
0	ADC_START	ADC scan enable register 0: ADC module does not scan; 1: ADC module starts scanning ADC_START is set from 0 to 1, ADC starts to scan, after scanning once, ADC_START hardware is automatically set to 0, corresponding to the ADC interrupt flag bit, the ADC interrupt flag bit needs to be cleared by software Note: ADC_START is not allowed to be configured during scanning

ADCCKC (B6H) ADC clock control register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-		ADCCKV		ADCCK	
R/W	-	-	-	-	R/W		R/W	
Reset value	-	-	-	-	0	0	0	0

Bit number	Bit symbol	Description
7~4	--	Reserved
3~2	ADCCKV	ADC comparator offset cancellation analog input clock. 0: 12MHz 1: 6MHz 2: 3MHz 3: 2MHz
1~0	ADCCK	ADC clock selection. 0: 3MHz 1: 2MHz 2: 1.5MHz 3: 1MHz

IPL0 (B8H) Interrupt priority register 0

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	PT1	PX2	PT0	PX0
R/W	-	-	-	-	R/W	R/W	R/W	R/W
Reset value	-	-	-	-	0	0	0	0

Bit number	Bit symbol	Description
7~4	–	Reserved
3	PT1	TF1(Timer1 interrupt) priority selection bit. 0: TF1(Timer1 interrupt) is low priority. 1: TF1(Timer1 interrupt) is high priority.
2	PX2	INT_EXT1 interrupt priority selection bit. 0: INT_EXT1 is low priority. 1: INT_EXT1 is high priority.
1	PT0	TF0(Timer0 interrupt) priority selection bit. 0: TF0(Timer0 interrupt) is low priority. 1: TF0(Timer0 interrupt) is high priority.
0	PX0	INT_EXT0 interrupt priority selection bit. 0: INT_EXT0 is low priority. 1: INT_EXT0 is high priority.

ADC_RDATAH (B9H) ADC scan result register high 4 bits

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	ADC_RDATAH [3:0]			
R/W	-	-	-	-	R			
Reset value	-	-	-	-	0			

Bit number	Bit symbol	Description
3~0	ADC_RAWDATAH [3:0]	ADC scan result register

ADC_RDATAL(BAH) ADC scan result register low 8 bits

Bit number	7	6	5	4	3	2	1	0
Symbol	ADC_RDATAL[7:0]							
R/W	R							
Reset value	0							

Bit number	Bit symbol	Description
7~0	ADC_RDATAL[7:0]	ADC scan result register

ADC_CFG1(BBH) ADC sampling timing control register 1

Bit number	7	6	5	4	3	2	1	0
Symbol	ADCWNUM					SAMBG	SAMDEL	
R/W	R/W					R/W	R/W	
Reset value	0					0	0	

Bit number	Bit symbol	Description
7~3	ADCWNUM	Selection of distance conversion interval time after sampling: (3+ADCWNUM)* t_{ADCK}
2	SAMBG	Sampling timing and comparison timing interval selection

		0: interval 0; 1: Interval 1* t_{ADCK}
1~0	SAMDEL	Sampling delay time selection 0: 0* t_{ADCK}; 1: 2* t_{ADCK}; 2: 4* t_{ADCK}; 3: 8* t_{ADCK}

ADC_CFG2 (BCH) ADC sampling timing control register 2

Bit number	7	6	5	4
Symbol	-	-	VREF_IN_ADC_SEL	
R/W	-	-	R/W	R/W
Reset value	-	-	0	0
Bit number	3	2	1	0
Symbol	FILTER_R_SEL	ADC_I_SEL		CTRL_SEL
R/W	R/W	R/W	R/W	R/W
Reset value	0	1	1	1

Bit number	Bit symbol	Description
5~4	VREF_IN_ADC_SEL	Input to ADC26 reference voltage selection 00: 1.378V; 01: 2.271V; 10: 3.168V; 11: 4.06V Need to read ADC internal channel input voltage calibration value when using
3	FILTER_R_SEL	Input signal filter selection 0: No RC filter added; 1: Add RC filter
2	ADC_I_SEL[1]	Op amp bias current selection signal 0: 1μA; 1: 2μA
1	ADC_I_SEL[0]	Comparator bias current selection signal 0: 1μA; 1: 2μA
0	CTRL_SEL	ADC comparator offset cancellation selection signal 00: First sampling and then offset elimination; 01: All switches are disconnected together

UART0_BDL (BDH) UART0 Baudrate control register

Bit number	7	6	5	4	3	2	1	0
Symbol	-							
R/W	R/W							
Reset value	0							

Bit number	Bit symbol	Description

7~0	--	Baud rate control register. Baud rate modules divisor register lower 8 bits, bandrate={UART0_BDH[1:0], UART0_BDL}, bandrate=0, does not generate baud rate clock. bandrate=1~1023, UART0 bandrate = BUSCLK/(16xBaud_Mod)

UART0_CON1 (BEH) UART0 control register 1

Bit number	7	6	5	4
Symbol	UART0_ ENABLE	TRANS_ ENABLE	RECEIVE_ ENABLE	MULTI_ MODE
R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0
Bit number	3	2	1	0
Symbol	STOP_MODE	DATA_MODE	PARITY_EN	PARITY_SEL
R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0

Bit number	Bit symbol	Description
7	UART0_ENABLE	Module enable. 1: module enable; 0: module off.
6	TRANS_ENABLE	Transmitter enable 1: transmitter is on; 0: transmitter is off
5	RECEIVE_ENABLE	Receiver enable. 1: receiver open; 0: receiver off.
4	MULTI_MODE	Multiprocessor communication mode. 1: mode enable; 0: mode disable.
3	STOP_MODE	Stop bit width selection. 1: 2 bit; 0: 1 bit.
2	DATA_MODE	Data mode select. 1: 9bit mode; 0: 8bit mode.
1	PARITY_EN	Parity enable. 1: parity enable; 0: parity disable.
0	PARITY_SEL	Parity select. 1: odd parity;

		0: even parity.

UART0_CON2 (BFH) UART0 control register 2

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	PAD_CHANGE	TX_EMPTY_IE	RX_FULL_IE	UART0_BDH	
R/W	-	-	-	R/W	R/W	R/W	R/W	
Reset value	-	-	-	0	1	1	0	0

Bit number	Bit symbol	Description
4	PAD_CHANGE	TXD/RXD pin interchange 1: pin interchange; 0: the pins are not interchangeable
3	TX_EMPTY_IE	Send interrupt enable. 1: interrupt enable; 0: interrupt disable (used in polling mode)
2	RX_FULL_IE	Received interrupt enable 1: interrupt enable; 0: interrupt disable (used in polling mode)
1~0	UART0_BDH	Baud rate modulus divisor register high 2bit.

UART0_STATE (C0H) UART0 status flag register

Bit number	7	6	5	4
Symbol	-	UART0_R8	UART0_T8	TI0
R/W	-	R	R/W	R/W
Reset value	-	0	0	0
Bit number	3	2	1	0
Symbol	RI0	UART0_RO	UART0_F	UART0_P
R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0

Bit number	Bit symbol	Description
6	UART0_R8	Receiver’s ninth data, read only.
5	UART0_T8	Transmitter’s ninth data, read only when parity is enabled.
4	TI0	Send interrupt flag. 1: send buffer is empty; 0: send buffer is full, software write 0 clear 0, write 1 invalid.
3	RI0	Receive interrupt flag. 1: receive buffer is full; 0: receive buffer is empty, software write 0 clear 0, write 1 invalid.

2	UART0_RO	Receive overflow flag; 1: receive overflow (lost new data); 0: no overflow, software write 0 clear 0, write 1 invalid.
1	UART0_F	Framing error flag. 1: framing error flag; 0: no framing error flag, software write 0 clear 0, write 1 invalid.
0	UART0_P	Parity error flag. 1: receiver parity error; 0: parity is correct, software write 0 clear 0, write 1 invalid.

UART0_BUF (C1H) UART0 data register

Bit number	7	6	5	4	3	2	1	0
Symbol	-							
R/W	R/W							
Reset value	FF							

Bit number	Bit symbol	Description
7~0	--	Data register Read returns read-only receive data buffer contents, write into write-only send data buffer.

COM_IO_SEL (C2H) COM port selection configuration register

Bit number	7	6	5	4	3	2	1	0
Symbol	COM7	COM6	COM5	COM4	COM3	COM2	COM1	COM0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Bit number	Bit symbol	Description
7~0	--	COM port selection configuration register, corresponding to PB port 1: Select COM port mode; 0: select IO port mode

ODRAIN_EN (C3H) PA0/PA1/PD6 port open-drain output enable register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	-	-	-
R/W	-	-	-	-	-	R/W	R/W	R/W
Reset value	-	-	-	-	-	0	0	0

Bit number	Bit symbol	Description
2~0	--	PA0/PA1/PD6 open-drain output enable register,

		corresponding to bit selection Bit[0]: PA0, Bit[1]: PA1, Bit[2]: PD6 1: Open drain output; 0: CMOS output

BOR_SEL(C4H) BOR control register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	PD_BOR	SEL_BOR_VTH		
R/W	-	-	-	-	R/W	R/W	R/W	R/W
Reset value	-	-	-	-	1	0	0	0

Bit number	Bit symbol	Description
3	PD_BOR	BOR control register 1: close; 0: open, close by default Note: it is recommended to open BOR when the program is first initialized, and open BOR without delay
2~0	SEL_BOR_VTH	BOR threshold selection 000: reserved; 001: 2.8V; 010: 3.3V; 011: 3.7V; 1xx: 4.2V

The BOR_SEL register is reset to 0x08 after power-on, and other resets will not change the configuration value.

UART1_BDL(C5H) UART1 baud rate control register

Bit number	7	6	5	4	3	2	1	0
Symbol	-							
R/W	R/W							
Reset value	0							

Bit number	Bit symbol	Description
7~0	-	Baud rate control register The lower 8 bits of the baud rate modulus divisor register, Baud_Mod={UART1_BDH[1:0], UART1_BDL}, When Baud_Mod=0, the baud rate clock is not generated, when Baud_Mod=1~1023, the baud rate = BUSCLK/(16xBaud_Mod)

UART1_CON1 (C6H) UART1 control register 1

Bit number	7	6	5	4
Symbol	UART1_ ENABLE	TRANS_ ENABLE	RECEIVE_E NABLE	MULTI_ MODE
R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0

Bit number	3	2	1	0
Symbol	STOP_MODE	DATA_MODE	PARITY_EN	PARITY_SEL
R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0

Bit number	Bit symbol	Description
7	UART1_ENABLE	Module enable 1: module enable; 0: module close
6	TRANS_ENABLE	Transmitter enable 1: transmitter is on; 0: transmitter is off
5	RECEIVE_ENABLE	Receiver enable 1: receiver is on; 0: receiver is off
4	MULTI_MODE	Multiprocessor communication mode 1: mode enable; 0: mode disable
3	STOP_MODE	Stop bit width selection 1: 2 bits; 0: 1 bit
2	DATA_MODE	Data mode selection 1: 9-bit mode; 0: 8-bit mode
1	PARITY_EN	Parity check enable 1: parity check is enabled; 0: parity check is disabled
0	PARITY_SEL	Parity selection 1: odd parity; 0: even parity

UART1_CON2(C7H) UART1 control register 2

Bit number	7	6	5	4
Symbol	-	-	-	PAD_CHANGE
R/W	-	-	-	R/W
Reset value	-	-	-	0
Bit number	3	2	1	0
Symbol	TX_EMPTY_IE	RX_FULL_IE	UART1_BDH	
R/W	R/W	R/W	R/W	R/W
Reset value	1	1	0	0

Bit number	Bit symbol	Description
4	PAD_CHANGE	TXD/RXD pin interchange 1: pin interchange; 0: the pins are not interchangeable
3	TX_EMPTY_IE	Transmit interrupt enable

		1: interrupt enable; 0: interrupt disabled (used in polling mode)
2	RX_FULL_IE	Receive interrupt enable 1: interrupt enable; 0: interrupt disabled (used in polling mode)
1~0	UART1_BDH	Baud rate modulus divisor register high 2 bits

UART1_STATE (C8H) UART1 status flag register

Bit number	7	6	5	4
Symbol	-	UART1_R8	UART1_T8	TI1
R/W	-	R	R/W	R/W
Reset value	-	0	0	0
Bit number	3	2	1	0
Symbol	RI1	UART1_RO	UART1_F	UART1_P
R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0

Bit number	Bit symbol	Description
6	UART1_R8	The 9th data of the receiver, read only
5	UART1_T8	The 9th data of the transmitter, read only during parity check
4	TI1	Send buffer empty interrupt flag 1: The sending buffer is empty; 0: Send buffer is full, software write 0 to clear
3	RI1	Receive interrupt flag 1: The receive buffer is full; 0: Receive buffer is empty, software write 0 to clear
2	UART1_RO	Receive overflow flag 1: Receive overflow (new data is lost); 0: No overflow, software writes 0 to clear
1	UART1_F	Frame error flag 1: A frame error is detected; 0: No frame error is detected, software writes 0 to clear
0	UART1_P	Parity error flag 1: Receiver parity error; 0: Parity check is correct, software writes 0 to clear

UART1_BUF (C9H) UART1 data register

Bit number	7	6	5	4	3	2	1	0
Symbol	-							
R/W	R/W							
Reset value	FF							

Bit number	Bit symbol	Description
7~0	-	Read returns the contents of the read-only receive data buffer, writes to the write-only send data buffer.

CSD_START(CAH) CSD scan open register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	-	-	-
R/W	-	-	-	-	-	-	-	R/W
Reset value	-	-	-	-	-	-	-	0

Bit number	Bit symbol	Description
0	-	1: CSD scanning is on; 0: CSD scan stops Write 1 in CSD_START to start scanning. After one scan, the hardware will automatically set to 0. If you want to start the next scan, you need to set it to 1 again by software; if CSD_START=0 during the scan, the scan will stop immediately, and the module will have related internal signals Reset Note: Must be used in accordance with the process configuration: CSD_START=1, if interruption is detected, configure CSD_START=0. CSD_START is not allowed to be configured during scanning

SNS_SCAN_CFG1 (CBH) Touch key scan configuration register 1

Bit number	7	6	5	4	3	2	1	0
Symbol	-	SW_PRE_OFF	PRS_DIV					
R/W	-	R/W	R/W					
Reset value	-	0	0					

Bit number	Bit symbol	Description
6	SW_PRE_OFF	Front-end charge and discharge clock switch control. 1: close sw_clk; 0: open sw_clk
5~0	PRS_DIV	Front-end charge and discharge clock frequency selection register: 0~61: fixed frequency: F=F48M/2/(PRS_DIV+4) (6M~369k); 62: highest frequency 3M, lowest frequency 1M, center frequency 1.5M, normal distribution; 63: highest frequency 3M, lowest frequency 1M, center frequency 1.5M, evenly distributed.

SNS_SCAN_CFG2 (CCH) Touch key scan configuration register 2

Bit number	7	6	5	4	3	2	1	0
Symbol	-	PULL_I_SELA_H	PARALLEL_EN	CSD_ADDR				
R/W	-	R/W	R/W	R/W				
Reset value	-	1	0	0				

Bit number	Bit symbol	Description
6	PULL_I_SELA_H	CSD pull-up current source configuration highest bit.
5	PARALLEL_EN	SNS channel shunt enable register. 1: reserved; 0: signal channel.
4~0	CSD_ADDR	The address of the detection channel 0~29 corresponds to the channel number 0~29

SNS_SCAN_CFG3(CDH) Touch key scan configuration register 3

Bit number	7	6	5	4	3	2	1	0
Symbol	-	RESO			CSD_DS		PRE_CHRG_SEL	INIT_DISCHRG_SEL
R/W	-	R/W			R/W		R/W	R/W
Reset value	-	1	1	1	0	0	0	0

Bit number	Bit symbol	Description
6~4	RESO	Counter bit select register. 000: 9 bits; 001: 10 bits; 010: 11 bits; 011: 12bits; 100: 13 bits; 101: 14 bits; 110: 15 bits; 111: 16 bits.
3~2	CSD_DS	Count clock frequency selection register. 00: 24M; 01: 12M; 10: 6M; 11: 4M; default 0.
1	PRE_CHRG_SEL	Pre-charge time selection 0: 20μs; 1: 40μs.
0	INIT_DISCHRG_SEL	Pre-discharge time selection 0: 2μs; 1: 10μs.

CSD_RAWDATAL (CEH) CSD counter, low 8-bit

Bit number	7	6	5	4	3	2	1	0
Symbol	CSD_RAWDATAL[7:0]							
R/W	R							
Reset value	0							

CSD_RAWDATAH (CFH) CSD counter, high 8-bit

Bit number	7	6	5	4	3	2	1	0
Symbol	CSD_RAWDATAH[7:0]							
R/W	R							

Reset value	0

PSW(D0H) Program status register

Bit number	7	6	5	4	3	2	1	0
Symbol	CY	AC	F0	RS[1:0]		OV	F1	P
R/W	R/W	R/W	R/W	R/W		R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Bit number	Bit symbol	Description
7	CY	Carry flag. Set when the addition generates a carry or subtracts a borrow, otherwise clears. Set when the first operand of CJNE is less than the second operand, cleared by MUL or DIV instruction. Also affected by mouse commands (RLC, RRC) and bitwise instructions.
6	AC	Auxiliary carry flag Set when the addition is borrowed from the third to fourth bits of the accumulator, or when the subtraction is borrowed from the third to fourth bits, otherwise cleared.
5	F0	0 flag bit. Universal label for users.
4~3	RS[1:0]	Working register group: Select a valid working register group: RS[1:0] Bank IRAM Area 00 0 0x00-0x07; 01 1 0x08-0x0F; 10 2 0x10-0x17; 11 3 0x18-0x1F
2	OV	Overflow flag bit When the addition produces a different carry of accumulator bits 6 and 7, or subtraction produces a borrow of accumulator bits 6 and 7, otherwise cleared. The OV flag indicates that the signed 8-bit result is out of bounds (greater than 127 or less than -128). The overflow flag is also set when the multiplication result is greater than 255 or an attempt is made to divide by 0.
1	F1	1 flag bit. Universal label for users.
0	P	Parity flag. Always contains the sum of Form 2 of all the bits in the accumulator.

PULL_I_SELA_L (D1H) CSD pull-up current source selection register

Bit number	7	6	5	4	3	2	1	0

Symbol	PULL_I_SEL<7:0>
R/W	R/W
Reset value	0

Bit number	Bit symbol	Description
7~0	PULL_I_SEL<7:0>	CSD pull up current source size selection switch. The default is 0.

SNS_ANA_CFG (D2H) CSD scan parameter configuration register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	RB_SEL			VTH_SEL		
R/W	-	-	R/W			R/W		
Reset value	-	-	1	0	1	1	0	1

Bit number	Bit symbol	Description
5~4	RB_SEL	Rb resistance size selection. 100: 60k; 101: 80k; Other: reserved Need to read Rb80K calibration value from chip flash when using: CBYTE [0x41CD] K/80K, proportional calculation normalization sensitivity.
2~1	VTH_SEL	VTH voltage selection signal 000: reserved; 001: 2.1V; 010: 2.5V; 011: 2.9V; 100: 3.2V; 101: 3.5V; 110: 3.9V; 111: 4.2V.

SNS_IO_SEL1(D3H) SNS channel select register 1

Bit number	7	6	5	4	3	2	1	0
Symbol	SNS_IO_SEL1 [7:0]							
R/W	R/W							
Reset value	0							

Bit number	Bit symbol	Description
7~0	SNS_IO_SEL1 [7:0]	SNS_IO_SEL1 [7: 0] corresponding to SNS7 ~ SNS0, the corresponding bit is 1: select SENSOR enable; 0: do not select SENSOR enable

SNS_IO_SEL2 (D4H) SNS channel select register 2

Bit number	7	6	5	4	3	2	1	0
Symbol	SNS_IO_SEL2 [7:0]							
R/W	R/W							

Reset value	0

Bit number	Bit symbol	Description
7~0	SNS_IO_SEL2[7:0]	SNS_IO_SEL2[7:0] corresponding to SNS15 ~ SNS8, the corresponding bit is enable 1: Select SENSOR; 0: Do not select SENSOR

SNS_IO_SEL3 (D5H) SNS channel select register 3

Bit number	7	6	5	4	3	2	1	0
Symbol	SNS_IO_SEL3 [7:0]							
R/W	R/W							
Reset value	0							

Bit number	Bit symbol	Description
7~0	SNS_IO_SEL3 [7:0]	SNS_IO_SEL3 [7:0] corresponding to SNS23 ~ SNS16, the corresponding bit is enable 1: Select SENSOR; 0: Do not select SENSOR

SNS_IO_SEL4 (D6H) SNS channel select register 4

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-					SNS_IO_SEL4[1:0]	
R/W	-	-					R/W	
Reset value	-	-					0	

Bit number	Bit symbol	Description
1~0	SNS_IO_SEL4[1:0]	SNS_IO_SEL4[1:0] corresponding to SNS25~ SNS24, the corresponding bit is enable 1: Select SENSOR; 0: Do not select SENSOR

RST_STAT (D7H) Reset flag register

Bit number	7	6	5	4	3	2	1	0
Symbol	BOOT_F	DEBUG_F	SOFT_F	PROG_F	ADDROF_F	BO_F	PO_F	WDTRST_F
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	1	0

Bit number	Bit symbol	Description
7	BOOT_F	0: No effect; 1: IAP operation BOOT upgrade reset occurred
6	DEBUG_F	0: No effect;

		1: Trim configuration reset occurred
5	SOFT_F	0: No effect; 1: Software reset occurred
4	PROG_F	0: No effect; 1: A programming reset occurred
3	ADDROF_F	0: No effect; 1: PC pointer overflow reset occurred
2	BO_F	0: No effect; 1: Power-down reset occurred
1	PO_F	0: No effect; 1: Brown-out reset occurred
0	WDTRST_F	0: No effect; 1: Watchdog timer overflow reset occurred

PD_PB(D8H) PB port pull-down resistor control register

Bit number	7	6	5	4	3	2	1	0
Symbol	PD_PB7	PD_PB6	PD_PB5	PD_PB4	PD_PB3	PD_PB2	PD_PB1	PD_PB0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Bit number	Bit symbol	Description
7~0	PD_PBn (n=7~0)	PB port pull-down resistor control register 1: The pull-down resistor is enabled; 0: The pull-down resistor is not enabled

ADC_IO_SEL1 (D9H) ADC function selection register 1

Bit number	7	6	5	4	3	2	1	0
Symbol	ADC_IO_SEL1[7:0]							
R/W	R/W							
Reset value	0							

Bit number	Bit symbol	Description
7~0	ADC_IO_SEL1[7:0]	ADC_IO_SEL1 [7: 0] corresponding to ADC07 ~ ADC00, the corresponding bit is 1: Select ADC function; 0: Do not select ADC function

ADC_IO_SEL2(DAH) ADC function selection register 2

Bit number	7	6	5	4	3	2	1	0
Symbol	ADC_IO_SEL2[7:0]							
R/W	R/W							
Reset value	0							

Bit number	Bit symbol	Description
7~0	ADC_IO_SEL2[7:0]	ADC_IO_SEL2 [7: 0] corresponding to ADC15 ~ ADC08, the corresponding bit is 1: Select ADC function; 0: Do not select ADC function

ADC_IO_SEL3(DBH) ADC function selection register 3

Bit number	7	6	5	4	3	2	1	0
Symbol	ADC_IO_SEL3[7:0]							
R/W	R/W							
Reset value	0							

Bit number	Bit symbol	Description
7~0	ADC_IO_SEL3[7:0]	ADC_IO_SEL3 [7: 0] corresponding to ADC23 ~ ADC16, the corresponding bit is 1: Select ADC function; 0: Do not select ADC function

ADC_IO_SEL4(DCH)ADCfunction selection register 4

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	-	ADC_IO_SEL4[1:0]	
R/W	-	-	-	-	-	-	R/W	
Reset value	-	-	-	-	-	-	0	

Bit number	Bit symbol	Description
1~0	ADC_IO_SEL4[1:0]	ADC_IO_SEL4 [1: 0] corresponding to ADC25 ~ ADC24, the corresponding bit is 1: Select ADC function; 0: Do not select ADC function

PU_PA (DDH) PA port pull-up resistor control register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	-	PU_PA1	PU_PA0
R/W	-	-		-	-	-	R/W	R/W
Reset value	-	-		-	-	-	0	0

Bit number	Bit symbol	Description
1~0	PU_PAn n=1~0	Port PA pull-up resistor enable register 1: The pull-up resistor is enabled; 0: The pull-up resistor is not enabled

PU_PB(DEH)PB port pull-up resistor control register

Bit number	7	6	5	4	3	2	1	0
Symbol	PU_PB7	PU_PB6	PU_PB5	PU_PB4	PU_PB3	PU_PB2	PU_PB1	PU_PB0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Bit number	Bit symbol	Description
7~0	PU_PBn n=1~0	Port PB pull-up resistor enable register 1: The pull-up resistor is enabled; 0: The pull-up resistor is not enabled

PU_PC(DFH) PC port pull-up resistor control register

Bit number	7	6	5	4	3	2	1	0
Symbol	PU_PC7	PU_PC6	PU_PC5	PU_PC4	PU_PC3	PU_PC2	PU_PC1	PU_PC0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Bit number	Bit symbol	Description
7~0	PU_PCn n=7~0	PC port pull-up resistor enable register 1: The pull-up resistor is enabled; 0: The pull-up resistor is not enabled

ACC(E0H) Accumulator

Bit number	7	6	5	4	3	2	1	0
Symbol	ACC							
R/W	R/W							
Reset value	0							

Bit number	Bit symbol	Description
7~0	ACC	Accumulator The targe register is suitable for all arithmetic and logic operations.

IRCON2 (E1H) Interrupt flag register 2

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	IE11	IE10	IE9	IE8
R/W	-	-	-	-	R/W	R/W	R/W	R/W
Reset value	-	-	-	-	0	0	0	0

Bit number	Bit symbol	Description
7~4	--	Reserved
3	IE11	External interrupt 3 interrupt flag 1: There is a INT3 interrupt flag;

		0: No INT3 interrupt flag
2	IE10	UART1 interrupt flag 1: There is a UART1 interrupt flag; 0: No UART1 interrupt flag
1	IE9	UART0 interrupt flag 1: There is a UART0 interrupt flag; 0: No UART0 interrupt flag
0	IE8	LVDT interrupt flag 1: There is a LVDT interrupt flag; 0: No LVDT interrupt flag

PU_PD (E2H) PD port pull-up resistor control register

Bit number	7	6	5	4	3	2	1	0
Symbol	PU_PD7	PU_PD6	PU_PD5	PU_PD4	PU_PD3	PU_PD2	PU_PD1	PU_PD0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Bit number	Bit symbol	Description
7~0	PU_PDn n=7~0	PD port pull-up resistor enable register 1: The pull-up resistor is enabled; 0: The pull-up resistor is not enabled

IICADD (E3H) IIC address register

Bit number	7	6	5	4	3	2	1	0
Symbol	IICADD[7:1]							-
R/W	R/W							-
Reset value	0							-

IICBUF (E4H) IIC transmit and receive data register

Bit number	7	6	5	4	3	2	1	0
Symbol	IICBUF							
R/W	R/W							
Reset value	0							

Bit number	Bit symbol	Description
7~0	IICBUF	IIC transmit receive data buffer

IICCON (E5H) IIC configuration register

Bit number	7	6	5	4
Symbol	–	–	IIC_RST	RD_SCL_EN
R/W	–	–	R/W	R/W
Reset value	–	–	0	1
Bit number	3	2	1	0

Symbol	WR_SCL_EN	SCLEN	SR	IIC_EN
R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0

Bit number	Bit symbol	Description
7~6	--	Reserved
5	IIC_RST	IIC module reset signal 1: IIC module reset operation 0: IIC module works properly
4	RD_SCL_EN	Host read pull low clock line control bit. 1: enable the host to read and pull the low clock line function; 0: disable the host to read and pull the low clock line function.
3	WR_SCL_EN	Host write pull low clock line control bit. 1: enable the host to write and pull the low clock line function; 0: disable the host to write and pull the low clock line function.
2	SCLEN	IIC clock enable bit 1: clock work properly 0: pull down the clock line.
1	SR	IIC conversion rate control bit 1: conversion rate control is turned off to adapt to the standard speed mode (100K); 0: conversion rate control is enabled to adapt to fast speed mode (400K)
0	IIC_EN	IIC work enable bit 1: IIC normal work; 0: IIC not work

IEN1 (E6H) Interrupt enable register 1

Bit number	7	6	5	4	3	2	1	0
Symbol	EX7	EX6	EX5	EX4	EX3	EX2	-	-
R/W	R/W	R/W	R/W	R/W	R/W	R/W	-	-
Reset value	0	0	0	0	0	0	-	-

Bit number	Bit symbol	Description
7	EX7	WDT/Timer2 interrupt enable 1: interrupt enable; 0: interrupt disable
6	EX6	LED interrupt enable 1: interrupt enable; 0: interrupt disable
5	EX5	CSD interrupt enable 1: interrupt enable; 0: interrupt disable
4	EX4	ADC interrupt enable

		1: interrupt enable; 0: interrupt disable
3	EX3	IIC interrupt enable 1: interrupt enable; 0: interrupt disable
2	EX2	External interrupt 2 interrupt enable 1: interrupt enable; 0: interrupt disable
1~0	-	Reserved

IEN2(E7H) Interrupt enable register 2

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	EX11	EX10	EX9	EX8
R/W	-	-	-	-	R/W	R/W	R/W	R/W
Reset value	-	-	-	-	0	0	0	0

Bit number	Bit symbol	Description
7~4	-	Reserved
3	EX11	External interrupt 3 interrupt enable 1: interrupt enable; 0: interrupt disable
2	EX10	UART1 interrupt enable 1: interrupt enable; 0: interrupt disable
1	EX9	UART0 interrupt enable 1: interrupt enable; 0: interrupt disable
0	EX8	LVDT interrupt enable 1: interrupt enable; 0: interrupt disable

IICSTAT (E8H) IIC status register

Bit number	7	6	5	4
Symbol	IIC_START	IIC_STOP	IIC_RW	IIC_AD
R/W	R	R	R	R
Reset value	0	1	0	0
Bit number	3	2	1	0
Symbol	IIC_BF	IIC_ACK	IIC_WCOL	IIC_RECOV
R/W	R	R	R/W	R/W
Reset value	0	1	0	0

Bit number	Bit symbol	Description
7	IIC_START	Start signal flag 1: boot bit detected; 0: no boot bit detected

6	IIC_STOP	Stop signal flag 1: stop status detected; 0: no stop status detected
5	IIC_RW	Read and write flag. Record the read/write information obtained from the address byte after the last address match. 1: read; 0: write.
4	IIC_AD	Address data flag bit. 1: indicates that the most recently received or sent byte is data; 0: indicates that the most recently received or sent byte is address.
3	IIC_BF	IICBUF full flag. Received in IIC bus mode: 1: received successfully, buffer is full; 0: received successfully, buffer is empty. Send in IIC bus mode: 1: data transmission is in progress (does not include the acknowledge bit and the stop bit), buffer is full; 0: data transmission has been completed (does not include the acknowledge bit and the stop bit), buffer is empty.
2	IIC_ACK	Answer flag 1: invalid response signal; 0: effective response signal.
1	IIC_WCOL	Write conflict flag. 1: when the IIC is transmitting the current data, the new data is attempted to be written to the transmit buffer; new data cannot be written to the buffer. 0: no write conflict
0	IIC_RECOV	Receive overflow flag bit 1: When the previous data received by the IIC has not been taken, new data is received, the new data cannot be received by the buffer. 0: no receive overflow.

IICBUFFER (E9H) IIC transmit and receive data buffer register

Bit number	7	6	5	4	3	2	1	0
Symbol	IICBUFFER							
R/W	R/W							
Reset value	0							

TRISA (EAH) PA port direction register

Bit number	7	6	5	4	3	2	1	0

Symbol	-	-	-	-	-	-	-	-
R/W	-	-	-	-	-	-	R/W	R/W
Reset value	-	-	-	-	-	-	1	1

Bit number	Bit symbol	Description
1~0	--	PA direction register, 0: output; 1: input

TRISB(EBH) PB port direction register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	-	-	-
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	1	1	1	1	1	1	1	1

Bit number	Bit symbol	Description
7~0	--	PB direction register, 0: output; 1: input

TRISC(ECH) PC port direction register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	-	-	-
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	1	1	1	1	1	1	1	1

Bit number	Bit symbol	Description
7~0	--	PC direction register, 0: output; 1: input

TRISD(EDH) PD port direction register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	-	-	-
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	1	1	1	1	1	1	1	1

Bit number	Bit symbol	Description
7~0	--	PD direction register, 0: output; 1: input

UART_IO_SEL(EEH) UART select enable register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	UART1_IO_SEL		UART0_IO_SEL		
R/W	-	-	-	R/W	R/W	R/W	R/W	R/W
Reset value	-	-	-	0	0	0	0	0

Bit number	Bit symbol	Description
4~3	UART1_IO_SEL	UART1 port selection enable 00: PB1/2 (RXD1_A/TXD1_A) port select UART1 function 01: PB6/7 (RXD1_B/TXD1_B) port select UART1 function 1x: PD4/5 (RXD1_C/TXD1_C) port select UART1 function
2~0	UART0_IO_SEL	UART0 port selection enable 000: PA0/1 (RXD0_A/TXD0_A) port select UART0 function 001: PB3/4 (RXD0_B/TXD0_B) port select UART0 function 010: reserved 011: PC0/1 (RXD0_D/TXD0_D) port select UART0 function 100: PD6/PA1 (RXD0_E/TXD0_E) port select UART0 function 101: PD7/PA0 (RXD0_F/TXD0_F) port select UART0 function

PWM0_IO_SEL (EFH) PWM0 select IO port configuration register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	PWM0_IO_SEL[3:0]			
R/W	-	-	-	-	R/W	R/W	R/W	R/W
Reset value	-	-	-	-	0	0	0	0

Bit number	Bit symbol	Description
3~0	PWM0_IO_SEL[3:0]	0: PB0 port; 1: PB1 port; 2: PB2 port; 3: PB3 port 4: PB5 port; 5: PC0 port; 6: PC3 port; 7: PC5 port; 8: PC6 port; 9: PC7 port

B (F0H) B register

Bit number	7	6	5	4	3	2	1	0
Symbol	B							
R/W	R/W							
Reset value	0							

Bit number	Bit symbol	Description
7~0	B	B register: the source and destination registers of multiplication and division operations.

IRCON1 (F1H) Interrupt flag register 1

Bit number	7	6	5	4	3	2	1	0
Symbol	IE7	IE6	IE5	IE4	IE3	IE2	-	-
R/W	R/W	R/W	R/W	R/W	R/W	R/W	-	-
Reset value	0	0	0	0	0	0	-	-

Bit number	Bit symbol	Description
7	IE7	WDT/Timer2 interrupt flag 1: There is a WDT/Timer2 interrupt flag; 0: No WDT/Timer2 interrupt flag
6	IE6	LED interrupt flag 1: There is a LED interrupt flag; 0: No LED interrupt flag
5	IE5	CSD interrupt flag 1: There is a CSD interrupt flag; 0: No CSD interrupt flag
4	IE4	ADC interrupt flag 1: There is a ADC interrupt flag; 0: No ADC interrupt flag
3	IE3	IIC interrupt flag 1: There is a IIC interrupt flag; 0: No IIC interrupt flag
2	IE2	External interrupt 2 interrupt flag 1: There is a INT2 interrupt flag; 0: No INT2 interrupt flag
1~0	-	Reserved

PERIPH_IO_SEL (F2H) IIC /INT function control register

Bit number	7	6	5	4	3
Symbol	-	IIC_AFIL_SEL	IIC_DFIL_SEL	IIC_IO_SEL	
R/W	-	R/W	R/W	R/W	R/W
Reset value	-	1	0	0	0
Bit number	2	1	0	/	
Symbol	INT2_IO_SEL	INT1_IO_SEL	INT0_IO_SEL	/	
R/W	R/W	R/W	R/W		
Reset value	0	0	0		

Bit number	Bit symbol	Description
6	IIC_AFIL_SEL	IIC port analog filter selection enable 1: select analog filter function; 0: do not select analog filter function.
5	IIC_DFIL_SEL	IIC port digital filter selection enable. 1: select digital filter function; 0: do not select digital filter function.
4~3	IIC_IO_SEL	IIC select enable 0: PA0/PA1 select IIC function; 1: PB5/PC0 select IIC function; 2: PA1/PD6 select IIC function (When PB5/PC0 is used as IIC port, there is no SR control function, automatic logic control becomes open-drain output, when PB5/PC0 is used as GPIO, there is no open-drain output function)
2	INT2_IO_SEL	INT2 select enable, correspond PD7 1: select INT2 function 0: not select INT2 function
1	INT1_IO_SEL	INT1 select enable, correspond PD6 1: select INT1 function 0: not select INT1 function
0	INT0_IO_SEL	INT0 select enable, correspond PD0 1: select INT0 function 0: not select INT0 function

IPL2 (F4H) Interrupt priority register 2

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	IPL2.3	IPL2.2	IPL2.1	IPL2.0
R/W	-	-	-	-	R/W	R/W	R/W	R/W
Reset value	-	-	-	-	0	0	0	0

Bit number	Bit symbol	Description
7~4	--	Reserved
3	IPL2.3	External interrupt 3 interrupt priority 0: low priority; 1: high priority
2	IPL2.2	UART1 interrupt priority. 0: low priority; 1: high priority
1	IPL2.1	UART0 interrupt priority. 0: low priority; 1: high priority
0	IPL2.0	LVDT interrupt priority. 0: low priority; 1: high priority

IPL1 (F6H) Interrupt priority register 1

Bit number	7	6	5	4	3	2	1	0
Symbol	IPL1.7	IPL1.6	IPL1.5	IPL1.4	IPL1.3	IPL1.2	-	-
R/W	R/W	R/W	R/W	R/W	R/W	R/W	-	-
Reset value	0	0	0	0	0	0	-	-

Bit number	Bit symbol	Description
7	IPL1.7	WDT/Timer 2 interrupt priority. 0: low priority; 1: high priority
6	IPL1.6	LED interrupt priority. 0: low priority; 1: high priority
5	IPL1.5	CSD interrupt priority. 0: low priority; 1: high priority
4	IPL1.4	ADC interrupt priority. 0: low priority; 1: high priority
3	IPL1.3	IIC interrupt priority. 0: low priority; 1: high priority
2	IPL1.2	External interrupt 2 priority. 0: low priority; 1: high priority
1~0	--	Reserved

EXT_INT_CON (F7H) External interrupt polarity control register

Bit number	7	6	5	4
Symbol	-	INT3_POLARITY	INT2_POLARITY	
R/W	-	R/W	R/W	R/W
Reset value	-	0	0	1
Bit number	3	2	1	0
Symbol	INT1_POLARITY		INT0_POLARITY	
R/W	R/W	R/W	R/W	R/W
Reset value	0	1	0	1

Bit number	Bit symbol	Description
6	INT3_POLARITY	External interrupt 3_x trigger polarity selection: 1: Rising edge (high level wake-up in idle mode 1) 0: Falling edge (low-level wake-up in idle mode 1)
5~4	INT2_POLARITY	External interrupt 2 trigger polarity selection: 01: Falling edge (low-level wake-up in idle mode 1) 10: rising edge (high level wake-up in idle mode 1) 00/11: Double edge (low-level wake-up in idle mode 1)
3~2	INT1_POLARITY	External interrupt 1 trigger polarity selection: 01: Falling edge (low-level wake-up in idle mode 1) 10: rising edge (high level wake-up in idle mode 1) 00/11: Double edge (low-level wake-up in idle mode 1)
1~0	INT0_POLARITY	External interrupt 0 trigger polarity selection: 01: Falling edge (low-level wake-up in idle mode 1) 10: rising edge (high level wake-up in idle mode 1) 00/11: Double edge (low-level wake-up in idle mode 1)

DATAA (F8H) PA data register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	-	PA1	PA0
R/W	-	-	-	-	-	-	R/W	R/W
Reset value	-	-	-	-	-	-	1	1

Bit number	Bit symbol	Description
1~0	--	PA data register. The output level of the PA group can be configured as the GPIO port. The read value is the level state of the current IO port (input) or the configured output (output) value.

SPROG_ADDR_H (F9H) Address control register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	-	-	-
R/W	-	-	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	-	-	0	0	0	0	0	0

Bit number	Bit symbol	Description
5~0	--	In non-FLASH BOOT upgrade mode, Bit[1:0] of this register is valid: Bit[1]: 0: select DATA area, 1: reserved; Bit[0]: High bit of the DATA area address, { SPROG_ADDR_H[0], SPROG_ADDR_L[7:0]} constitute

		the DATA area address In FLASH BOOT upgrade mode, Bit[5:0] of this register is valid: {SPROG_ADDR_H[5:0], SPROG_ADDR_L[7:0]} are multiplexed to address all spaces of CODE from 0x0000~0x3FFF

SPROG_ADDR_L(FAH) Address control register lower 8 bits

Bit number	7	6	5	4	3	2	1	0
Symbol	SPROG_ADDR_L[7:0]							
R/W	R/W							
Reset value	0							

Bit number	Bit symbol	Description
7~0	SPROG_ADDR_L[7:0]	lower 8 bits of address

SPROG_DATA(FBH) Data register

Bit number	7	6	5	4	3	2	1	0
Symbol	-							
R/W	R/W							
Reset value	0							

Bit number	Bit symbol	Description
7~0	--	data to be written

SPROG_CMD(FCH) Command register

Bit number	7	6	5	4	3	2	1	0
Symbol	-							
R/W	R/W							
Reset value	0							

Bit number	Bit symbol	Description
7~0	--	Write 0x96: page erase; Write 0x69: byte programming When continuously writing data 0x12, 0x34, 0x56, 0x78, 0x9a, enter the BOOT upgrade mode of Flash; When writing data 0xfe, 0xdc, 0xba, 0x98, 0x76 continuously, exit the BOOT upgrade mode of Flash; When CFG_BOOT_EN=1 or the program is running in a non-BOOT space, the BOOT upgrade mode cannot be entered

SPROG_TIM (FDH) Erase and write time control register

Bit number	7	6	5	4	3	2	1	0

Symbol	-	-	-	-	-	-	-	-
R/W	-	-	-	R/W	R/W	R/W	R/W	R/W
Reset value	-	-	-	1	1	0	1	0

Bit number	Bit symbol	Description
7~5	--	reserved
4~0	--	Byte write fixed time 62μs 0~20: erasing time=20 ms ~40ms (step 1ms); >20: Erase time=30ms

PD_ANA (FEH) Module switch control register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	LDO_ LOAD2	LDO_ LOAD1	XTAL_SEL	PD_XTAL	PD_CSD	PD_ADC
R/W	-	-	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	-	-	0	0	0	1	1	1

Bit number	Bit symbol	Description
7~6	-	Reserved
5	LDO_LOAD2	In Idle mode 0, DC load is controlled by 450μA, reset value is 0 0: 450μA with DC load; 1: No DC load
4	LDO_LOAD1	RTC crystal oscillator circuit control register 1: Select 4MHz; 0: Select 32768Hz
3	XTAL_SEL	RTC crystal oscillator circuit control register 1: Select 4MHz; 0: Select 32768Hz
2	PD_XTAL	RTC crystal oscillator circuit control register. 1: close; 0: open; default close.
1	PD_CSD	Analog CSD work control register: 0: CSD module works normally; 1: CSD module does not work
0	PD_ADC	Analog ADC shutdown control register 0: ADC module works normally; 1: ADC module does not work

LVDT_SEL (FFH) LVDT control register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	PD_LVDT	SEL_LVDT_VTH		

R/W	-	-	-	-	R/W	R/W	R/W	R/W
Reset value	-	-	-	-	1	0	0	0

Bit number	Bit symbol	Description
3	PD_LVDT	LVDT control register 1: close; 0: open, close by default
2~0	SEL_LVDT_VTH	LVDT threshold selection 000: reserved; 001: 3.0V; 010: 3.3V; 011: 3.6V; 100: 3.9 V; others: 4.2 V;

Note:

1. Reset value: reset value in different modes;

RST_STAT register power-on reset: rst_state is 0x02;

Reset in other modes: the reset flag bit corresponding to rst_state is 1, and other reset flags remain in their original state;

2. The reserved register and the reserved bits of the register are forbidden to write operation, otherwise the chip may be abnormal.

4.2. Secondary Bus Registers Detailed Description

CFG1_REG (01H) Configuration word register 1

Bit number	7	6	5	4	3	2	1	0
Symbol	-							
R/W	R							
Reset value	86							

CFG2_REG (02H) Configuration word register 2

Bit number	7	6	5	4	3	2	1	0
Symbol	-							
R/W	R							
Reset value	7F							

CFG3_REG (03H) Configuration word register 3

Bit number	7	6	5	4	3	2	1	0
Symbol	-							
R/W	R							
Reset value	FF							

CFG4_REG (04H) Configuration word register 4

Bit number	7	6	5	4	3	2	1	0
Symbol	-							
R/W	R							
Reset value	30							

CFG5_REG (05H) Configuration word register 5

Bit number	7	6	5	4	3	2	1	0
Symbol	-							
R/W	R							
Reset value	0F							

CFG6_REG (06H) Configuration word register 6

Bit number	7	6	5	4	3	2	1	0
Symbol	-							
R/W	R							
Reset value	1F							

CFG7_REG (07H) Configuration word register 7

Bit number	7	6	5	4	3	2	1	0
Symbol	-							
R/W	R							
Reset value	1F							

CFG8_REG (08H) Configuration word register 8

Bit number	7	6	5	4	3	2	1	0
Symbol	-							
R/W	R							
Reset value	7F							

CFG9_REG (09H) Configuration word register 9

Bit number	7	6	5	4	3	2	1	0
Symbol	-							
R/W	R							
Reset value	3F							

CFG30_REG (0AH) Configuration word register 30

Bit number	7	6	5	4	3	2	1	0
Symbol	-							
R/W	R							
Reset value	FF							

FLASH_BOOT_EN (21H) BOOT mode status register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	-	-	FLASH_BOOT_EN
R/W	-	-	-	-	-	-	-	R
Reset value	-	-	-	-	-	-	-	0

Bit number	Bit symbol	Description
0	FLASH_BOOT_EN	1: Enter Flash BOOT upgrade mode, 0: Exit Flash BOOT upgrade mode.

		Note: In this mode, SPROG_ADDR_H, SPROG_ADDR_L, SPROG_DATA, SPROG_CMD, SPROG_TIM are reused as the BOOT upgrade function. {SPROG_ADDR_H, SPROG_ADDR_L} are multiplexed into all Flash space addresses from 0x0000 to 0x7FFF.

BOOT_CMD (22H) Program space jump instruction register

Bit number	7	6	5	4	3	2	1	0
Symbol	-							
R/W	RW							
Reset value	0							

Bit number	Bit symbol	Description
7~0	--	Configure the program space jump instruction, write 5 groups of data (0xFF, 0x00, 0x88, 0x55, 0xAA) continuously, and jump into the main program space; Continuously write 5 groups of data (0x37, 0xC8, 0x42, 0x9A, 0x65), jump into the Boot program space; the value read out is the most recently written byte.

ROM_OFFSET_L (23H) Address offset of CODE area (low 8 bits)

Bit number	7	6	5	4	3	2	1	0
Symbol	-							
R/W	RO							
Reset value	0							

Bit number	Bit symbol	Description
7~0	--	Address offset of CODE area (low 8 bits)

ROM_OFFSET_H (24H) Address offset of CODE area (high 8 bits)

Bit number	7	6	5	4	3	2	1	0
Symbol	-							
R/W	RO							
Reset value	0							

Bit number	Bit symbol	Description
7~0	--	Address offset of CODE area (high 8 bits)

REG_ADDR (96H) Secondary bus address configuration register

Bit number	7	6	5	4	3	2	1	0
Symbol	-		REG_ADDR					
R/W	-		RW	RW	RW	RW	RW	RW
Reset value	-		0	0	0	0	0	0

Bit number	Bit symbol	Description
5~0	REG_ADDR	Secondary bus address configuration register When operating the secondary bus register, it is recommended to read and write the secondary bus register, first EA = 0, then EA = 1 after the operation is completed, to prevent other interrupts or operations from modifying the address or data of the secondary bus register

REG_DATA (97H) Secondary bus data read and write registers

Bit number	7	6	5	4	3	2	1	0
Symbol	REG_DATA							
R/W	RW							
Reset value	0							

Bit number	Bit symbol	Description
7~0	REG_DATA	Secondary bus data read and write registers It is recommended to read and write secondary bus registers, first EA = 0, and then EA = 1 after the operation is completed, to prevent other interrupts or operations from modifying the secondary bus register address or data

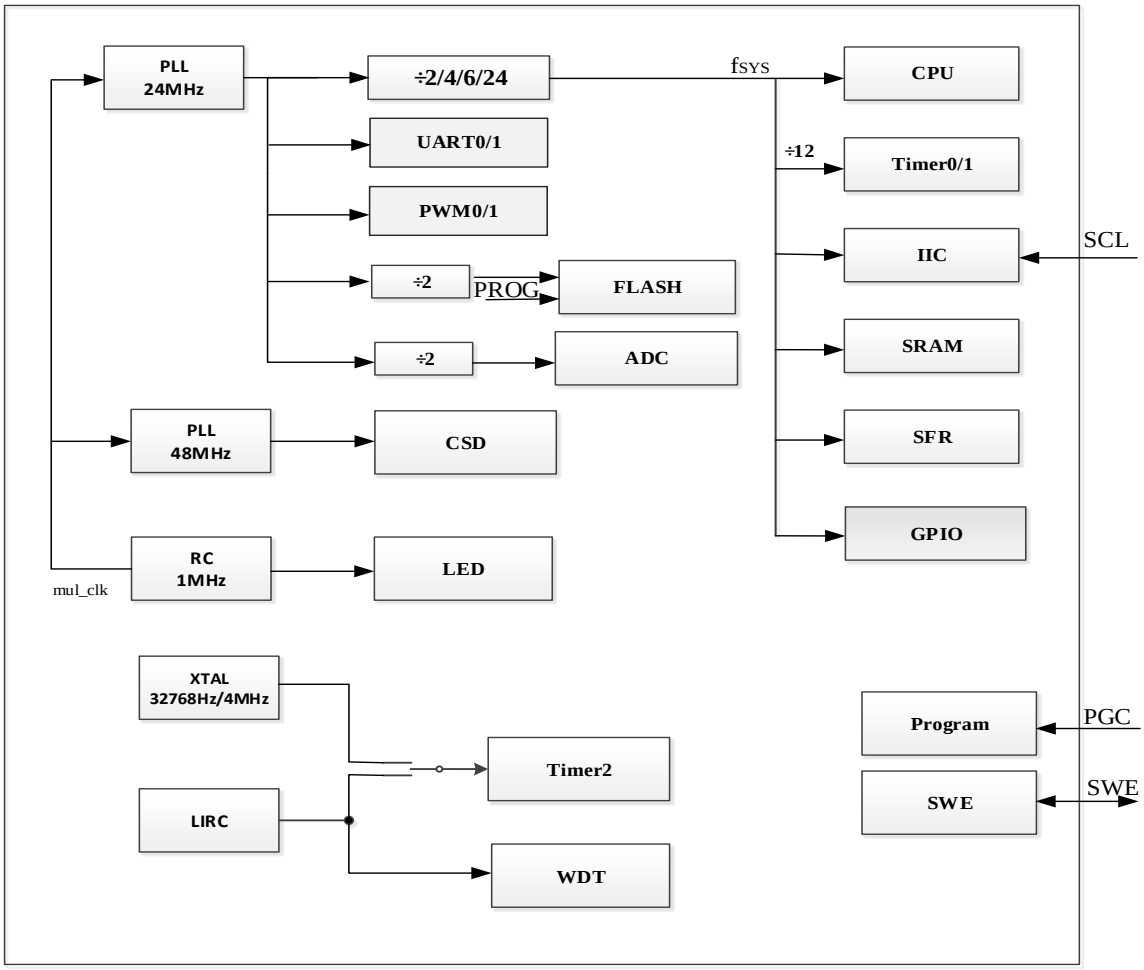
5. Clock, Reset, Work Mode, WDT

5.1. Clock

5.1.1. Clock Definition

Clock source:

- Internal high-speed RC oscillator: RC1M
- Internal low speed RC oscillator: LIRC32k
- External crystal oscillator: 32768 Hz/4 MHz
- RC1M multiplier to get PLL clock: PLL48M/ PLL24M



Clock block diagram

The BF7812AMXX-XJLX series clock is defined as follows:

RC1MHz: Built-in RC oscillator with a frequency of 1MHz, used as LED clock;

mul_clk: Multiply RC1M to get the PLL clock;

PLL_24MHz: The 24 MHz clock generated by the phase-locked loop is directly used for the control of UART, FLASH, etc., and the system clock is obtained after frequency division;

f_{SYS}: system clock 12 MHz/6 MHz /4 MHz /1 MHz, which can be used as core-related clock

PLL_48MHz: The 48MHz clock generated by the phase-locked loop, the clock source of CSD;
XTAL32768Hz/4MHz: External crystal oscillator 32768Hz/4MHz, mainly used for Timer2 clock;
LIRC: Internal low-speed clock 32kHz, which is used as watchdog clock and Timer2 clock;
SCL: IIC master clock, sent by the IIC master, as the IIC communication clock;
PGC: Programming clock, download clock when programming and burning programs;

5.1.2. Clock Registers

SYS_CLK_CFG (84H) Clock control register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	IM0_EN	PLL_CLK_SEL	
R/W	-	-	-	-	-	R/W	R/W	
Reset value	-	-	-	-	-	0	0	1

Bit number	Bit symbol	Description
7~3	--	Reserved
1~0	PLL_CLK_SEL	PLL clock divided selection register 00: 12MHz; 01: 6MHz; 10: 4MHz; 11: 1MHz

TIMER2_CFG (93H) TIMER2 CFG register

Bit number	7~3	2	1	0
Symbol	-	TIMER2_CLK_SEL	TIMER2_RLD	TIMER2_EN
R/W	-	R/W	R/W	R/W
Reset value	-	0	0	0

Bit number	Bit symbol	Description
7~3	--	reserved
2	TIMER2_CLK_SEL	TIMER2 clock select register 1: select XTAL 32768Hz/4MHz 0: select LIRC

PD_ANA (FEH) Module switch control register

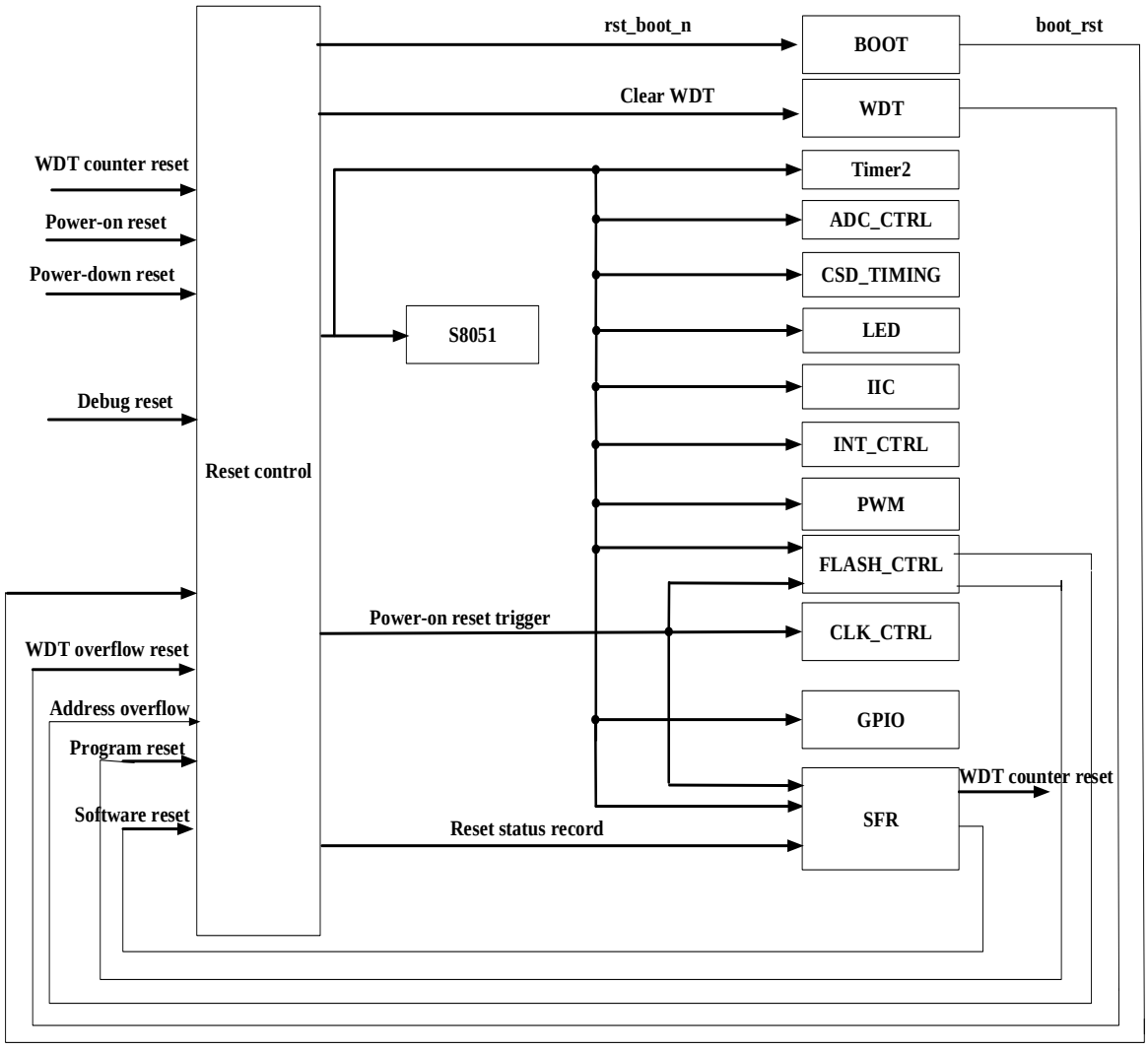
Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	LDO_ LOAD2	LDO_ LOAD1	XTAL_SEL	PD_XTAL	PD_CSD	PD_ADC
R/W	-	-	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	-	-	0	0	0	1	1	1

Bit number	Bit symbol	Description

7~6	-	Reserved
5	LDO_LOAD2	In Idle mode 0, DC load is controlled by 450μA, reset value is 0 0: 450μA with DC load; 1: No DC load
4	LDO_LOAD1	RTC crystal oscillator circuit control register 1: Select 4MHz; 0: Select 32768Hz
3	XTAL_SEL	RTC crystal oscillator circuit control register 1: Select 4MHz; 0: Select 32768Hz
2	PD_XTAL	RTC crystal oscillator circuit control register. 1: close; 0: open; default close.

5.2. Reset

There are 8 reset modes in BF7812AMXX-XJLX: WDT overflow reset (WDTRST_F), power on reset (PO_F), brown-out reset (BO_F), program reset (PROG_F), debug reset (DEBUG_F), PC pointer overflow reset (ADDROF_F), software reset (SOFT_F), IAP operation BOOT upgrade reset (BOOT_F). Any one of above reset, global will make chip reset. We can judge the reset flag register which reset happen, the reset must be cleared by software.



Reset block diagram

5.2.1. Reset sequence

po_n: power-on reset: The analog module generates a low level signal after the system is powered up and lasts for 93ms. When Power-on reset is low, the entire chip is in the reset state, after goes to high, the global reset signal will continue effective 20ms, the system exits reset mode.

bo_n: brown-out reset, the analog module generates a low level signal after a power down reset occurs in the system. When Power-down reset is low, the entire chip is in the reset state, after goes to high, the global reset signal will continue effective 20ms, system exits reset mode.

prog_en: Programming reset. When prog_en is high, it is the programming mode of FLASH. At this time, the global reset signal is valid. After it goes low, the global reset signal continues to be valid for 20ms.

soft_rst: software reset, make the soft reset signal vaild by writing the SFR, so that the global reset signal is active 20ms. After 20ms, the system exits the reset mode.

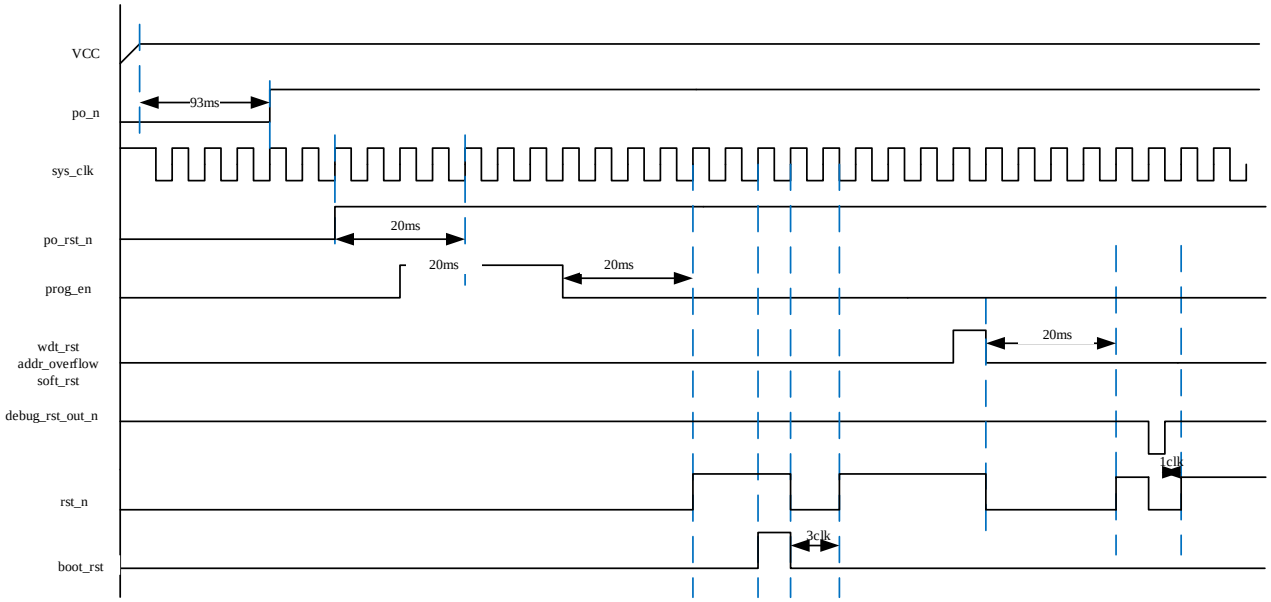
wdt_rst: WDT Overflow Reset, reset the global for 20ms after the WDT overflow. After 20ms, the system exits the reset mode.

addr_overflow: PC Pointer Overflow Reset, if the MCU addresses the program memory PC pointer beyond the flash valid address range, the addr_overflow signal goes high. The rising edge of the sys_clk detects the addr_overflow high level (need one clock cycle) and resets the global 20ms, the reset signal clears the addr_overflow signal. After 20ms, the system exits the reset mode.

debug_rst_out_n: debug Reset, for the core repair module output reset signal, low means reset is valid. Chip global reset, there will be no 20ms initialization process, only one system clock reset low.

boot_rst: BOOT address jump reset, after the complete ROM space jump instruction is configured, the boot_rst signal becomes high, and the sys_clk clock checks the boot_rst high level (valid for one clock cycle) to reset the global, but there will be no 20ms read configuration word process, only Delay the reset low level of 3 system clocks.

Reset sequence description:



1. The chip has a power-on reset, and the analog POR module delays for 93ms, and po_n is pulled high.

2. The programmer sends instructions to make the chip enter the programming mode (prog_en is pulled high), and exits the programming mode after completing the programming. After a delay of 20ms, rst_n is pulled high and the chip enters normal operation.

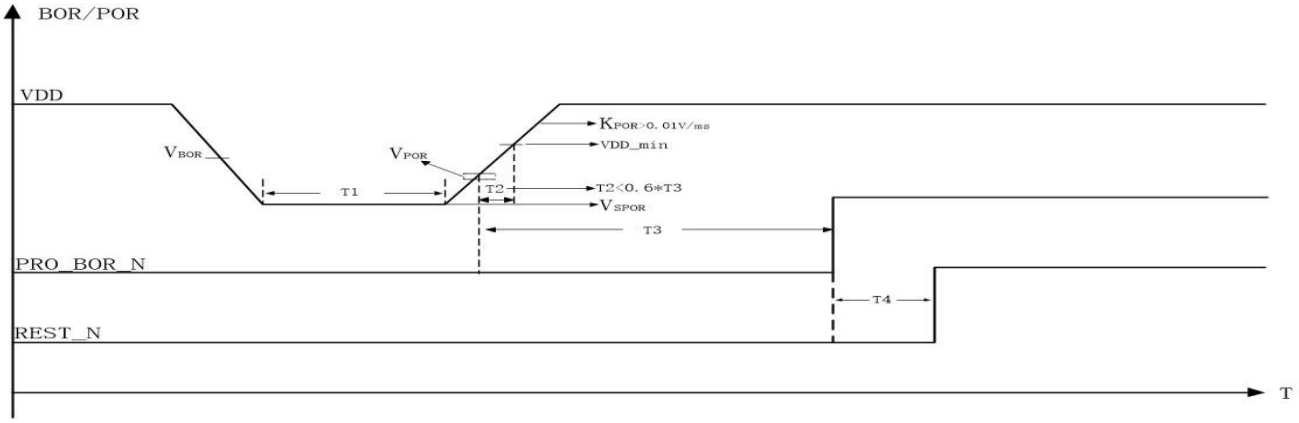
3. During normal operation, any one of watchdog reset, address overflow reset, and soft reset occurs, rst_n is pulled low, after a delay of 20ms, rst_n is pulled high, and the chip enters normal operation.

4. After normal work, you cannot enter the programming mode.

5. In debug mode, configure debug reset, pull down rst_n, pull up 1 system clock in debug_rst_out_n, pull up rst_n, and the chip enters normal operation.

6. When the chip supports the BOOT upgrade function, a ROM address jump reset occurs, rst_n is pulled low, and after 3 system clocks, rst_n is pulled high, and the chip enters normal operation.

Power-up/power-down sequence:



Power-on reset diagram

BOR/POR Parameters:

Symbol	Parameter	Test Conditions		Min	Typ	Max	Unit
		VCC	temperature				
V_{SPOR}	Power on reset start voltage	-	25℃	-	-	300	mV
K_{POR}	Power on reset voltage rate	-	25℃	0.01	-	-	V/ms
V_{POR}	Power on reset voltage	-	25℃	1.1	1.5	2.2	V
V_{BOR}	Brownout reset voltage (±10%), hysteresis 0.2V	-	25℃	-	V_{BOR}	-	V
VDD_min	Minimum operating voltage	-	25℃	2.7	-	-	V
T1	VDD keep VSPOR time	-	25℃	0.1	-	-	ms
T2	VPOR from VDD_min time	-	25℃	-	-	0.6*T3	ms
T3	Reset POR_BOR_N duration	-	25℃	55	93	131	ms
T4	Global reset effective time	-	25℃	-	20	-	ms

Power on reset parameter characteristic table

V_{BOR}: 2.8V; 3.3V; 3.7V; 4.2V.

When VDD is affected by the load or severely disturbed, if the voltage drops into the voltage dead zone and the chip is not within the working voltage range, it may cause the system to work abnormally, such as DATA area data loss. The function of power-down reset (BOR) is to monitor when VDD drops to the BOR voltage, the MCU can generate a power-down reset in advance to avoid system errors.

Suggestions to prevent entering the voltage dead zone and reduce the probability of system error:

- BOR is turned on when the program is first initialized, and BOR is turned on without delay
- Increase the voltage drop slope

5.2.2. Reset Registers

SFR				
Address	**Name**	**RW**	**Reset value**	**Description**
0xD7	RST_STAT	RW	0000_0010b②	Reset flag register
0x8E	SOFT_RST	RW	0000_0000b	Soft reset register
0xC4	BOR_SEL	RW	xxxx_1000b①	BOR control register

Note: '①': The reset value is the default value after power-on reset, and the value after the global reset is completed is the factory calibration value.

'②': The power-on reset value is 0x02, and the reset flag bit corresponding to other reset values is 1. The other reset flag bits remain in their original state.

RST_STAT (D7H) Reset flag register

Bit number	7	6	5	4	3	2	1	0
Symbol	BOOT_F	DEBUG_F	SOFT_F	PROG_F	ADDROF_F	BO_F	PO_F	WDTRST_F
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	1	0

Bit number	Bit symbol	Description
7	BOOT_F	0: No effect; 1: IAP operation BOOT upgrade reset occurred
6	DEBUG_F	0: No effect; 1: Trim configuration reset occurred
5	SOFT_F	0: No effect; 1: Software reset occurred
4	PROG_F	0: No effect; 1: A programming reset occurred
3	ADDROF_F	0: No effect; 1: PC pointer overflow reset occurred
2	BO_F	0: No effect; 1: Brown-out reset occurred
1	PO_F	0: No effect; 1: Power-on reset occurred
0	WDTRST_F	0: No effect; 1: Watchdog timer overflow reset occurred

Note: Reset value, reset value in different modes. Example: Power-on reset: rst_state is 0x02; other mode reset: the reset flag bit corresponding to rst_state is 1, and other reset flags remain in their original state.

SOFT_RST(8EH) Soft reset register

Bit number	7	6	5	4	3	2	1	0
Symbol	-							

R/W	R/W
Reset value	0

Bit number	Bit symbol	Description
7~0	--	Software reset register. Software reset is only generated when the register value is 0x55.

BOR_SEL(C4H) BOR control register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	PD_BOR	SEL_BOR_VTH		
R/W	-	-	-	-	R/W	R/W	R/W	R/W
Reset value	-	-	-	-	1	0	0	0

Bit number	Bit symbol	Description
3	PD_BOR	BOR control register 1: close; 0: open, close by default Note: it is recommended to open BOR when the program is first initialized, and open BOR without delay
2~0	SEL_BOR_VTH	BOR threshold selection 000: reserved; 001: 2.8V; 010: 3.3V; 011: 3.7V; 1xx: 4.2V

The BOR_SEL register is reset to 0x08 after power-on, and other resets will not change the configuration value.

Threshold selection SEL_BOR_VTH	BOR			
	brown-out voltage threshold (V)	Recovery threshold (V)	Hysteresis (mV)	Delay(μs)
001	2.8	3.0	223	81.0
010	3.3	3.5	188	106.3
011	3.7	3.9	235	124.5
1XX	4.2	4.4	199	147.1

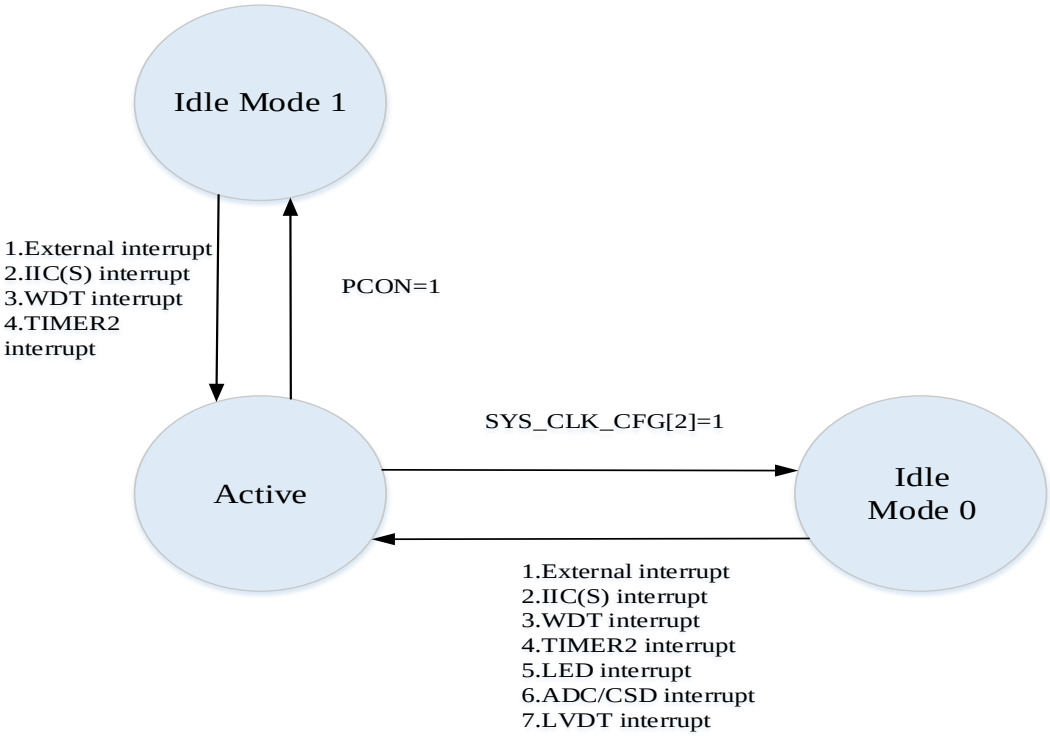
5.3. Working Mode

5.3.1. Introduction

BF7812AMXX-XJLX series working mode: active mode, standby mode.

BF7812AMXX-XJLX provides SYS_CLK_CFG register, configure Bit2 of this register to control MCU to enter idle mode 0. BF7812AMXX-XJLX provides PCON register, configure Bit0 of this register to control MCU to enter idle mode 1.

- **Active Mode**
  RC1M, PLL, LIRC work, XTAL depends on software configuration. The core runs, the peripherals keep working normally, and the functions of each peripheral are controlled by software configuration.
- **Standby mode is divided into idle mode 0 and idle mode 1**
  - **Idle Mode 0**
    RC1M, PLL, LIRC work, XTAL depends on software configuration. The core stops running, the UART, PWM peripherals do not work, and the rest of the peripherals can work.
  - **Idle Mode 1**
    RC1M and PLL are off, LIRC works, XTAL depends on software configuration. The core is stopped and the peripherals work fine using the LIRC clock.



Working mode conversion diagram

Ways to exit Idle Mode 0:

- Enable any one of IIC, External Interrupt0, External Interrupt1, External Interrupt2, External Interrupt 3, WDT, Timer2, LED, CSD, ADC, LVDT can wake up the chip, exit the Idle Mode 0, and the CPU executes the interrupt service routine.

Ways to exit Idle Mode 1:

- Enable IIC, External Interrupt0, External Interrupt1, External Interrupt2, External Interrupt 3, WDT, Timer2, any of them can wake up the chip and exit the Idle Mode 1. After the interrupt response is generated, the CPU executes the interrupt service routine related to the interrupt vector. And after the RETI return instruction is executed, it returns to the next instruction that causes the CPU to enter the Idle Mode 1 to continue running the program.

Note: PCON = 0x01, BOR off can obtain lower power consumption, but the chip needs to ensure that it is in the normal operating voltage range (2.7V~5.5V), if the chip power supply is unstable, resulting in less than 2.7V, it is strongly recommended that BOR be turned on.

Mode	Contions	Effect on the clock	
Active Mode	Wake-up from power-on reset/standby mode	LIRC	work
		XTAL32K/4M	Depends on software configuration
		RC1M	work
		PLL	work
Idle Mode 0	SYS_CLK_CFG[2] =1	LIRC	work
		XTAL32K/4M	Depends on software configuration
		RC1M	work
		PLL	work
Idle Mode 1	PCON=1	LIRC	work
		XTAL32K/4M	Depends on software configuration
		RC1M	close
		PLL	close

Working status table of clock source in each mode

NO	Module Name	Clock source	Work status		
			Active Mode	Idle Mode 0	Idle Mode 1
1	s8051	f_{SYS}	√	×	×
2	UART0~1	PLL_24M	According Configuration	×	×
3	PWM0~2	PLL_24M	According Configuration	×	×
4	Internal Timer0	f_{SYS}	According Configuration	×	×

5	Internal Timer1	f_{SYS}	According Configuration	×	×
6	External Timer2	LIRC/ XTAL32K/4MHz	According Configuration	According Configuration	According Configuration
7	LED	RC1M	According Configuration	According Configuration	×
8	WDT	LIRC	According Configuration	According Configuration	According Configuration
9	ADC_CTRL	PLL_12M	According Configuration	According Configuration	×
10	CSD_Timing	PLL_48M	According Configuration	According Configuration	×
11	IIC(S)	f_{SYS}	According Configuration	According Configuration	According Configuration

Status table for each digital module in different modes

5.3.2. Registers

SYS_CLK_CFG (84H) Clock control register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	IM0_EN	PLL_CLK_SEL	
R/W	-	-	-	-	-	R/W	R/W	
Reset value	-	-	-	-	-	0	0	1

Bit number	Bit symbol	Description
2	IM0_EN	Idle Mode 0 enable 1: Enter Idle Mode 0; 0: Exit Idle Mode 0

PCON(87H) Idle mode 1 select register

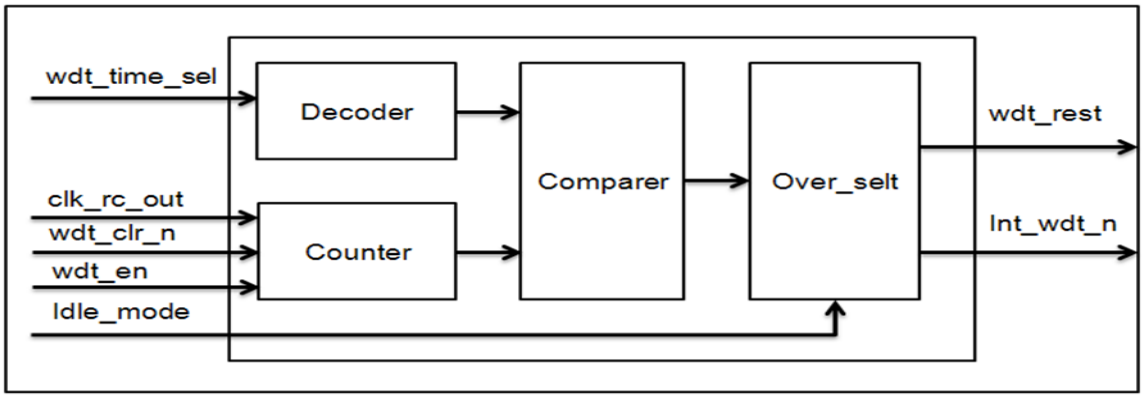
Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	-		IM1_EN
R/W	-	-	-	-	-	-	-	R/W
Reset value	-	-	-	-	-	-	-	0

Bit number	Bit symbol	Description
0	IM1_EN	Idle Mode 1 Enable 1: Idle mode 1; 0: Active mode, automatically cleared after wake-up Note: The software delay must be greater than or equal to 100 μs after wake-up, otherwise the wake-up function is abnormal

5.4. WDT

5.4.1. Introduction

The WDT timing counting circuit uses the internal low-speed clock LIRC for timing, and the configurable timing time is 2^n*18ms (n=0, 1, 2, 3, 4, 5, 6, 7)----- Here n is the configuration value of the timing configuration register.



Classification of WDT overflow signals due to the particularity of the system applications:

In normal mode, if the WDT overflow occurs, the overflow signal is the WDT overflow reset signal, the WDT overflow reset affects the global reset. At this point, the system implements a global reset action and reloads the configuration information.

In Idle mode 1, if the WDT overflow, the overflow signal is the WDT interrupt signal. Interrupt wake-up chip exits Idle mode 1 and executes WDT interrupt service function.

The watchdog module is a timing counting module. Its count clock is the internal low-speed clock LIRC. Its timing clear signal is composed of global reset and configuration clear. This signal is synchronously released by the watchdog timing clock in the reset module; The clearing action is generated every time the CPU configures the watchdog timer configuration register (WDT_CTRL), and the watchdog restarts timing; at the same time, the watchdog counter has the watchdog count enable control, when the count enable is valid, After the watchdog generates a timing overflow (reset or interrupt), as long as the watchdog counting enable is not turned off, the watchdog counter will restart counting.

5.4.2. WDT Registers

SFR register				
Address	**Name**	**RW**	**Reset value**	**Description**
0x85	INT_PE_STAT	RW	xxxx_xx00b	WDT/Timer2 interrupt status register
0x91	WDT_CTRL	RW	xxxx_x000b	WDT timing overflow control register
0x92	WDT_EN	RW	0000_0000b	WDT timing enable register
0xE6	IEN1	RW	0000_00xxb	Interrupt enable register 1
0xF1	IRCON1	RW	0000_00xxb	Interrupt flag register 1
0xF6	IPL1	RW	0000_00xxb	Interrupt priority register 1

WDT SFR list

INT_PE_STAT(85H)WDT/Timer2 interrupt status register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	-	INT_WDT_STAT	INT_TIMER2_STAT
R/W	-	-	-	-	-	-	R/W	R/W
Reset value	-	-	-	-	-	-	0	0

Bit number	Bit symbol	Description
1	INT_WDT_STAT	WDT interrupt status, set 0, write WDT_CTRL can set 0. 1: interrupt effective 0: invalid interrupt

WDT_CTRL(91H) WDT timing overflow control register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	WDT_TIME_SEL		
R/W	-	-	-	-	-	R/W		
Reset value	-	-	-	-	-	0	0	0

Bit number	Bit symbol	Description
7~0	WDT_TIME_SEL	WDT overflow timer register. Timing length is as follows: 0x00: 18ms; 0x01: 36ms; 0x02: 72ms; 0x03: 144ms; 0x04: 288ms; 0x05: 576ms; 0x06: 1152ms; 0x07: 2304ms;

The watchdog uses the internal low-speed clock LIRC to complete the timing function and can achieve timing from 18ms to 2.3s. The timing length is controlled by SFR (WDT_CTRL), as shown in the following table

WDT_EN(92H) WDT timing enable register

Bit number	7	6	5	4	3	2	1	0
Symbol	WDT_EN							
R/W	R/W							
Reset value	0							

Turn off WDT when writing 0x55, write other values to enable WDT, the WDT always works after the reset is over. Clearing the WDT is done by writing to the WDT_CTRL register. Whichever values is written to this register will clear the WDT.

IEN1 (E6H) Interrupt enable register 1

Bit number	7	6	5	4	3	2	1	0
Symbol	EX7	EX6	EX5	EX4	EX3	EX2	-	-
R/W	R/W	R/W	R/W	R/W	R/W	R/W	-	-
Reset value	0	0	0	0	0	0	-	-

Bit number	Bit symbol	Description
7	EX7	WDT/Timer2 interrupt enable 1: interrupt enable; 0: interrupt disable

IRCON1 (F1H) Interrupt flag register 1

Bit number	7	6	5	4	3	2	1	0
Symbol	IE7	IE6	IE5	IE4	IE3	IE2	-	-
R/W	R/W	R/W	R/W	R/W	R/W	R/W	-	-
Reset value	0	0	0	0	0	0	-	-

Bit number	Bit symbol	Description
7	IE7	WDT/Timer2 interrupt flag 1: there is a WDT/Timer2 interrupt flag; 0: no WDT/Timer2 interrupt flag

IPL1 (F6H) Interrupt priority register 1

Bit number	7	6	5	4	3	2	1	0
Symbol	IPL1.7	IPL1.6	IPL1.5	IPL1.4	IPL1.3	IPL1.2	-	-
R/W	R/W	R/W	R/W	R/W	R/W	R/W	-	-
Reset value	0	0	0	0	0	0	-	-

Bit number	Bit symbol	Description
7	IPL1.7	WDT/Timer 2 interrupt priority. 0: low priority; 1: high priority

6. GPIO

Some pins of the GPIO port are multiplexed with device peripheral functions, and cannot be configured as multiple clock functions at the same time, otherwise it will cause malfunction. IIC communication port, open-drain output, pull-up resister required.

TRISX register (Direction Register): TRISX set to 1 can be configured as input pin, set to 0 can be configured as output pin.

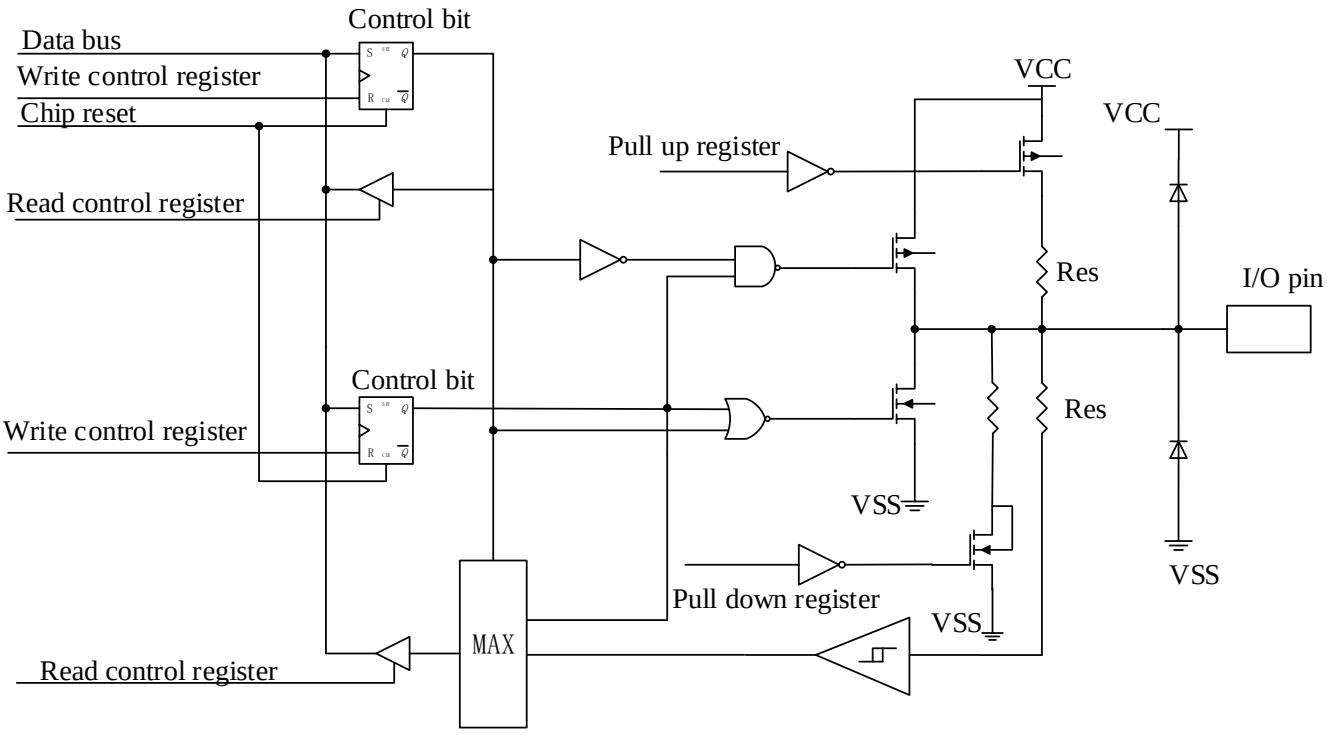
DATAX register (Data Register): DATAX set to 1 the data in DATAX will be configured as high, set to 0 the data in DATAX will be configured as low.

PU_PX register (Pull-up resistance control register): PU_PX set to 1 corresponding pin pull-up resistor enable, clear the corresponding pin does not enable pull-up resistor, and pull-up resistor 4.7k (PB port pull-up resistor 30k).

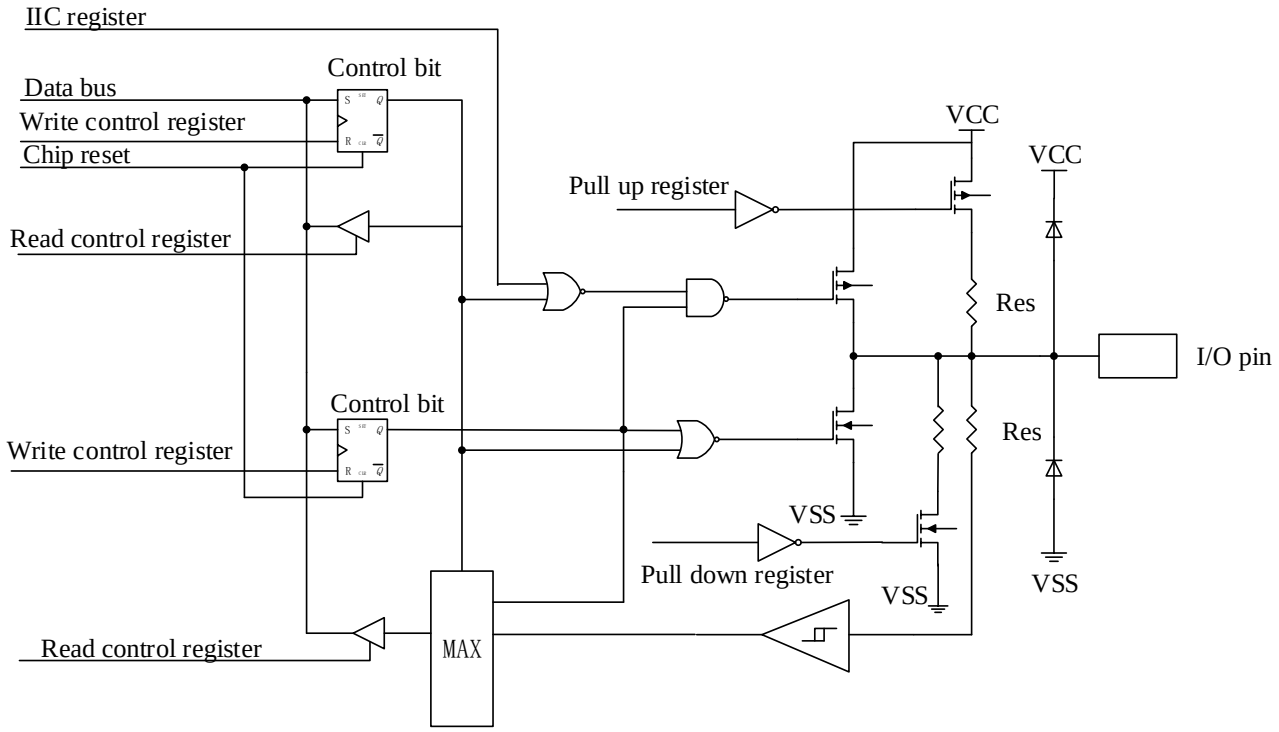
PD_PB register (PB pull-down resistor control register): Set PD_PB to 1 to enable the corresponding pin pull-down resistor, clear the corresponding pin to disable the pull-down resistor, built-in pull-down resistor 30k.

ODRAIN_EN register: ODRAIN_EN set to 1 corresponding pin will enable open drain output, set to 0 corresponding pin corresponding pin output disenabled, automatically turn on open-drain after enabling IIC function. IIC/UART recommends using external pull-up resistors.

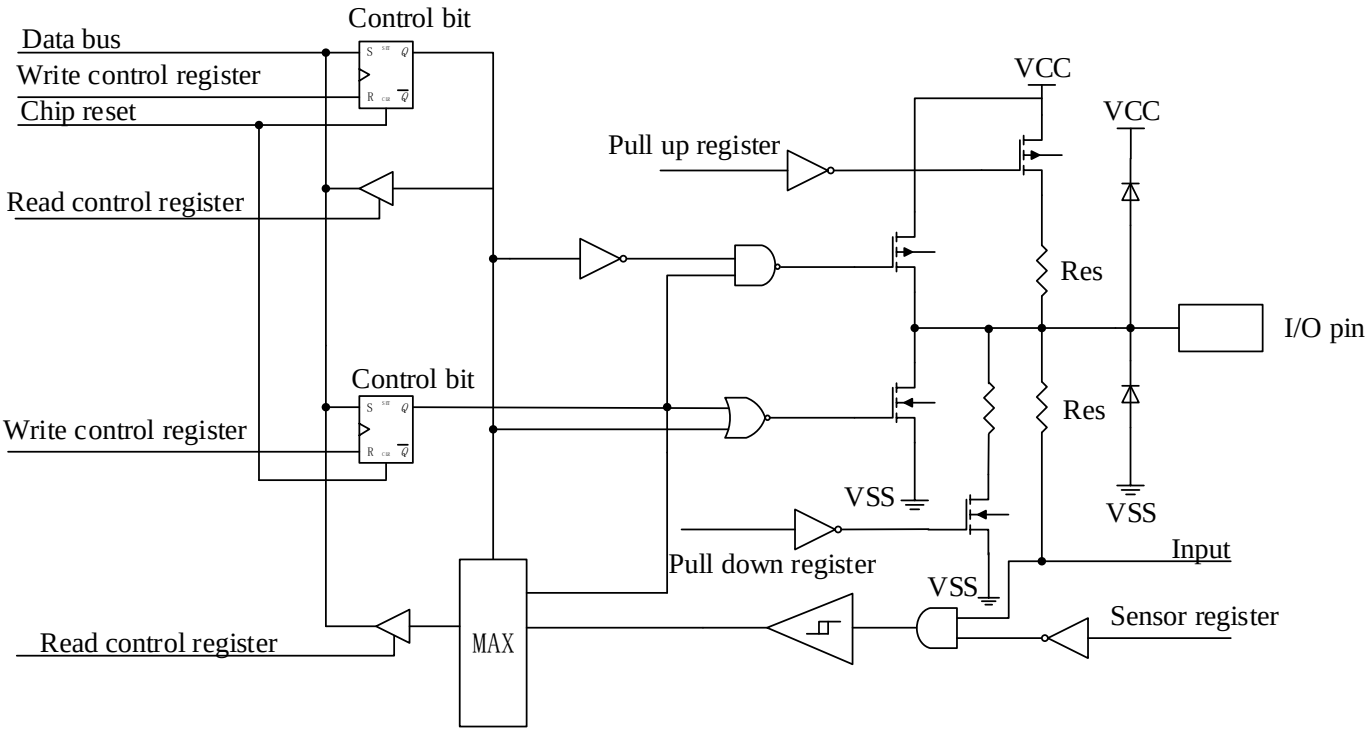
Supports 8 GPIO ports for high current drive functions.



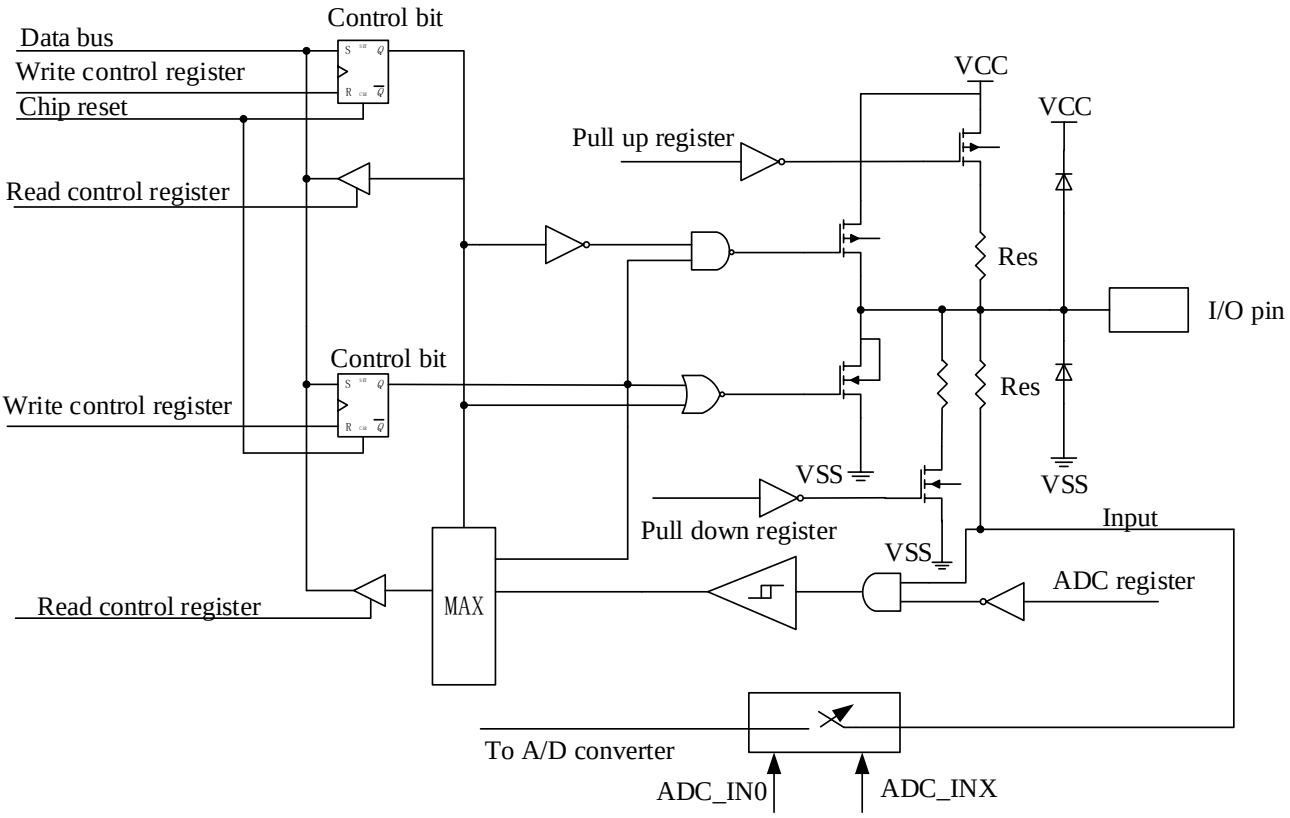
General IO structure



Open-drain output structure



SNS IO structure



ADC IO structure

6.1. GPIO Related Register

SFR register				
Address	**Name**	**RW**	**Reset value**	**Description**
0xF8	DATAA	RW	xxxx_xx11b	PA data register
0x80	DATAB	RW	1111_1111b	PB data register
0x90	DATAC	RW	1111_1111b	PC data register
0x98	DATAD	RW	1111_1111b	PD data register
0xB0	DP_CON	RW	xxx0_0000b	LED scan control register
0xC2	COM_IO_SEL	RW	0000_0000b	COM selection configuration register
0xC3	ODRAIN_EN	RW	xxxx_x000b	PA0/PA1/PD6 port open drain output enable register
0xD8	PD_PB	RW	0000_0000b	PB port pull-down resistor control register
0xDD	PU_PA	RW	xxxx_xx00b	PA port pull-up resistor control register
0xDE	PU_PB	RW	0000_0000b	PB port pull-up resistor control register
0xDF	PU_PC	RW	0000_0000b	PC port pull-up resistor control register
0xE2	PU_PD	RW	0000_0000b	PD port pull-up resistor control register
0xEA	TRISA	RW	xxxx_xx11b	PA direction register
0xEB	TRISB	RW	1111_1111b	PB direction register
0xEC	TRISC	RW	1111_1111b	PC direction register
0xED	TRISD	RW	1111_1111b	PD direction register

Port configuration SFR list

6.2. GPIO Register Detailed Description

6.2.1. Data Register

DATAA (F8H) PA data register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	-	PA1	PA0
R/W	-	-	-	-	-	-	R/W	R/W
Reset value	-	-	-	-	-	-	1	1

Bit number	Bit symbol	Description
1~0	--	PA data register. The output level of the PA group can be configured as the GPIO port. The read value is the level state of the current IO port (input) or the configured output (output) value.

DATAB(80H)PB data register

Bit number	7	6	5	4	3	2	1	0
Symbol	PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	1	1	1	1	1	1	1	1

Bit number	Bit symbol	Description
7~0	--	PB data register. The output level of the PB group can be configured as the GPIO port. The read value is the level state of the current IO port (input) or the configured output (output) value.

DATAC(90H) PC data register

Bit number	7	6	5	4	3	2	1	0
Symbol	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	1	1	1	1	1	1	1	1

Bit number	Bit symbol	Description
7~0	--	PC data register. The output level of the PC group can be configured as the GPIO port. The read value is the level state of the current IO port (input) or the configured output (output) value.

DATAD(98H) PD data register

Bit number	7	6	5	4	3	2	1	0
Symbol	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	1	1	1	1	1	1	1	1

Bit number	Bit symbol	Description
7~0	--	PD data register. The output level of the PD group can be configured as the GPIO port. The read value is the level state of the current IO port (input) or the configured output (output) value.

6.2.2. Pull-up resistor control register

PU_PA (DDH) PA port pull-up resistor control register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	-	PU_PA1	PU_PA0
R/W	-	-		-	-	-	R/W	R/W
Reset value	-	-		-	-	-	0	0

Bit number	Bit symbol	Description
1~0	PU_PAn n=1~0	Port PA pull-up resistor enable register 1: The pull-up resistor is enabled; 0: The pull-up resistor is not enabled

PU_PB(DEH)PB port pull-up resistor control register

Bit number	7	6	5	4	3	2	1	0
Symbol	PU_PB7	PU_PB6	PU_PB5	PU_PB4	PU_PB3	PU_PB2	PU_PB1	PU_PB0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Bit number	Bit symbol	Description
7~0	PU_PBn n=1~0	Port PB pull-up resistor enable register 1: The pull-up resistor is enabled; 0: The pull-up resistor is not enabled

PU_PC(DFH) PC port pull-up resistor control register

Bit number	7	6	5	4	3	2	1	0
Symbol	PU_PC7	PU_PC6	PU_PC5	PU_PC4	PU_PC3	PU_PC2	PU_PC1	PU_PC0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Bit number	Bit symbol	Description
7~0	PU_PCn	PC port pull-up resistor enable register

	n=7~0	1: The pull-up resistor is enabled; 0: The pull-up resistor is not enabled

PU_PD (E2H) PD port pull-up resistor control register

Bit number	7	6	5	4	3	2	1	0
Symbol	PU_PD7	PU_PD6	PU_PD5	PU_PD4	PU_PD3	PU_PD2	PU_PD1	PU_PD0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Bit number	Bit symbol	Description
7~0	PU_PDn n=7~0	PD port pull-up resistor enable register 1: The pull-up resistor is enabled; 0: The pull-up resistor is not enabled

6.2.3. Direction Register

TRISA (EAH) PA direction register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	-	-	-
R/W	-	-	-	-	-	-	R/W	R/W
Reset value	-	-	-	-	-	-	1	1

Bit number	Bit symbol	Description
1~0	--	PA direction register 0: output 1: input

TRISB(EBH) PB port direction register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	-	-	-
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	1	1	1	1	1	1	1	1

Bit number	Bit symbol	Description
7~0	--	PB direction register, 0: output; 1: input

TRISC(ECH) PC port direction register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	-	-	-
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	1	1	1	1	1	1	1	1

Bit number	Bit symbol	Description

7~0	--	PC direction register 0: output; 1: input

TRISD(EDH) PD port direction register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	-	-	-
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	1	1	1	1	1	1	1	1

Bit number	Bit symbol	Description
7~0	--	PD direction register 0: output 1: input

6.2.4. Large Current Sink

DP_CON (B0H) LED scan control register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	DUTY_SEL			SCAN_MODE	COM_MOD
R/W	-	-	-	R/W			R/W	R/W
Reset value	-	-	-	0	0	0	0	0

Bit number	Bit symbol	Description
0	COM_MOD	Large sink current ports drive enable. 1: COM port function lock, work as a large current IO port. 0: COM port function is not locked and can be configured as other functions. When the COM port locks the large sink current IO port, by configuring GPIO registers output drive timing, it is vaild when all of the following LED scan configurations are invalid.

COM_IO_SEL (C2H) COM port selection configuration register

Bit number	7	6	5	4	3	2	1	0
Symbol	COM7	COM6	COM5	COM4	COM3	COM2	COM1	COM0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Bit number	Bit symbol	Description
7~0	--	COM port selection configuration register, corresponding to PB port 1: select COM port mode; 0: select IO port mode

6.2.5. Open Drain Output Enable Register

ODRAIN_EN (2CH) PA0/PA1/PD6 port open drain output enable register(Secondary bus register)

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	-	-	-
R/W	-	-	-	-	-	R/W	R/W	R/W
Reset value	-	-	-	-	-	0	0	0

Bit number	Bit symbol	Description
2	--	PD6 open-drain output enable register 1: Open drain output; 0: CMOS output
1	--	PA1 open-drain output enable register 1: Open drain output; 0: CMOS output
0	--	PA0 open-drain output enable register 1: Open drain output; 0: CMOS output

6.2.6. Pull-down Resistor Enable Register

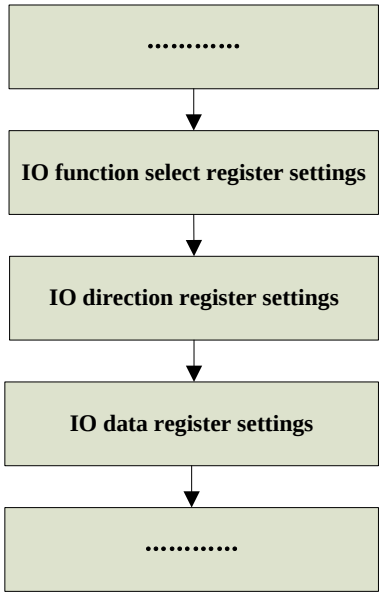
PD_PB(D8H) PB port pull-down resistor control register

Bit number	7	6	5	4	3	2	1	0
Symbol	PD_PB7	PD_PB6	PD_PB5	PD_PB4	PD_PB3	PD_PB2	PD_PB1	PD_PB0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Bit number	Bit symbol	Description
7~0	PD_PBn (n=7~0)	PB port pull-down resistor control register 1: The pull-down resistor is enabled; 0: The pull-down resistor is not enabled

6.3. GPIO Configuration Process

When setting the port to GPIO, the following three sets of registers need to be set accordingly.



IO configuration flow chart

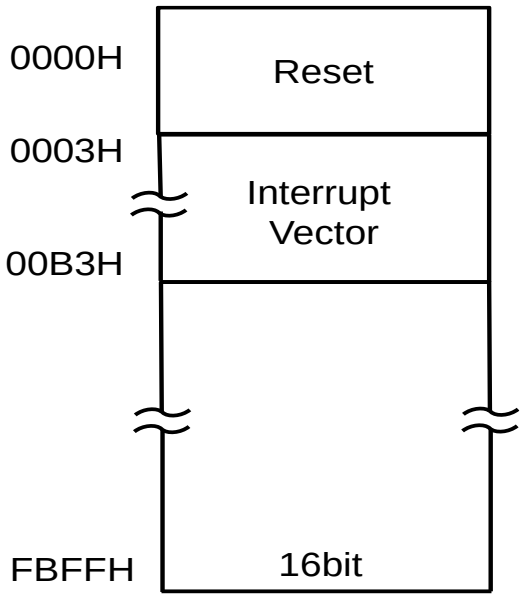
Note: The default source current drive capability of the IO port is typically 20mA, and the sink current drive capability is typically 50mA @5V 0.9VCC. When using IO to drive the LED/digital tube, you need to pay attention to the Ifp current of the LED lamp. It is recommended to add a current limiting resistor. The IO drive peak current is limited to the LED/digital tube Ifp current.

7. Interrupt

7.1. Interrupt Sources and Entry Address

Interrupt source	Condition	Sign	Enable control	Priority control	Interrupt vector	Query priority	Interrupt number	Flag removal method	wakeup idle mode 1
INT0	External interrupt 0 condition is met	IE0	IEN0[0]	IPL0[0]	0x0003	1	0	User must clear	Yes
Timer0	Timer0 overflow	TF0	IEN0[1]	IPL0[1]	0x000B	2	1	User must clear	No
INT1	External interrupt 1 condition is met	IE1	IEN0[2]	IPL0[2]	0x0013	3	2	User must clear	Yes
Timer1	Timer1 overflow	TF1	IEN0[3]	IPL0[3]	0x001B	4	3	User must clear	No
INT2	External interrupt 2 condition is met	IE2	IEN1[2]	IPL1[2]	0x004B	5	9	User must clear	Yes
IIC	Receive or send completed	IE3	IEN1[3]	IPL1[3]	0x0053	6	10	User must clear	Yes
ADC	ADC conversion completed	IE4	IEN1[4]	IPL1[4]	0x005B	7	11	User must clear	No
CSD	Counter overflow	IE5	IEN1[5]	IPL1[5]	0x0063	8	12	User must clear	No
LED	Scan complete	IE6	IEN1[6]	IPL1[6]	0X006B	9	13	User must clear	No
WDT/ Timer2	WDT/Timer2 overflow	IE7	IEN1[7]	IPL1[7]	0x0073	10	14	User must clear	Yes
LVDT	Voltage conditions meet	IE8	IEN2[0]	IPL2[0]	0x007B	11	15	User must clear	No
UART0	Receive or send completed	IE9	IEN2[1]	IPL2[1]	0x0083	12	16	User must clear	No
UART1	Receive or send completed	IE10	IEN2[2]	IPL2[2]	0x008B	13	17	User must clear	No
INT3	External interrupt 3 condition is met	IE11	IEN2[3]	IPL2[3]	0x0093	14	18	User must clear	No

List of interrupt information



When the chip generates a reset signal, the program starts from the 0x0000 address. When an interrupt signal occurs, the program will jump to the interrupt vector program address to execute the interrupt service routine.

7.2. Interrupt Function

7.2.1. Interrupt Response

When an interrupt request, CPU according to the interrupt vectors determine the type of interrupt service routine (ISR) to run. CPU complete execution ISR, unless a higher priority interrupt source applying for a break. After each ISR has RETI (return from interrupt) instruction. After RETI instruction, CPU continues to execute the program before the interrupt did not happen.

ISR can only be a higher priority interrupt request interrupt. That is, the low-priority ISR can be interrupted by a high-priority interrupt request.

The BF7812AMXX-XJLX responses interrupt request until the current instruction finished. If the RETI instruction is being executed or read IPL, IEN register, after an additional instruction then respond the interrupt request.

7.2.2. Interrupt Priority

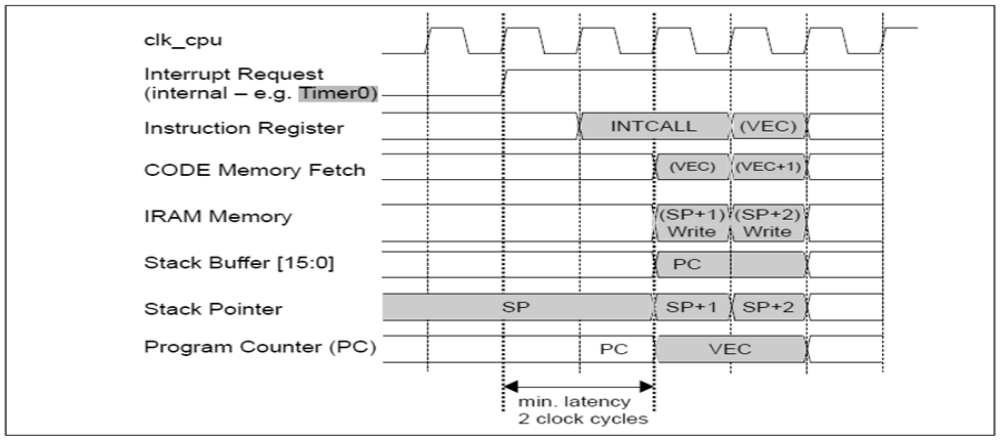
The BF7812AMXX-XJLX has two interrupt priority levels: interrupt level and default priority. Interrupt levels (highest, high, and low) take precedence over the default priority. The priority set to high is the first to respond. When the priority is set to the same level, the response will be queued by default. If allowed, the power-down interrupt is the only highest-level interrupt source. Other interrupt sources can be set to high priority or low priority.

Each interrupt source can be assigned a priority level (high or low), and the default priority. The same level of interrupt sources (such as both high priority) the priority is the default priority decision. Interrupt service routine in progress can only be a high-priority interrupt request interrupt.

7.2.3. Interrupt Sampling

Internal modules such as internal timers and serial ports generate interrupt requests through interrupt flag bits in their respective SFRs. At the end of first clock per instruction cycle (C1), at the rising edge of the external interrupt system clock sampling.

To ensure edge-triggered interrupt is detected, the corresponding port must maintain high level for two clocks and maintain low for level two clock.



Interrupt sampling timing diagram

7.2.4. Interrupt Wait

Interrupt response time is determined by current state. Fastest response time is five instruction cycles: one cycle to detect the interrupt request, the other 4 used to execute long call (LCALL) to ISR.

When the system is executing a RETI instruction and is followed by a MUL or DIV instruction, the interrupt waits for the longest time (13 instruction cycles). This 13 instruction cycles are as follows: one cycle to detect the interrupt request, three to complete the RETI, five used to execute DIV or MUL instruction, 4 used to execute long call (LCALL) to ISR. In this case, the response time is 13 clock cycles.

7.3. Interrupt Related Register

SFR register				
Address	**Name**	**RW**	**Reset value**	**Description**
0x85	INT_PE_STAT	RW	xxxx_xx00b	WDT/Timer2 interrupt status register
0x86	INT_POBO_STAT	RW	xxxx_xx00b	LVDT boost/LVDT buck interrupt status register
0x88	TCON	RW	0000_0x0xb	Timer control register
0xA8	IEN0	RW	0xxx_0000b	Interrupt enable register
0xAC	PERIPH_IO_SEL3	RW	x000_0000b	INT3 select enable register 3
0xAD	PERIPH_IO_SEL2	RW	0000_0000b	INT3 select enable register 2
0xAE	PERIPH_IO_SEL1	RW	0000_0000b	INT3 select enable register 1
0xB8	IPL0	RW	xxxx_0000b	Interrupt priority register 0
0xE1	IRCON2	RW	xxxx_0000b	Interrupt flag register 2
0xE6	IEN1	RW	0000_00xxb	Interrupt enable register 1
0xE7	IEN2	RW	xxxx_0000b	Interrupt enable register 2
0xF1	IRCON1	RW	0000_00xxb	Interrupt flag register 1
0xF2	PERIPH_IO_SEL	RW	x100_0000b	IIC /INT function control register
0xF4	IPL2	RW	xxxx_0000b	Interrupt priority register 2
0xF6	IPL1	RW	0000_00xxb	Interrupt priority register 1
0xF7	EXT_INT_CON	RW	x001_0101b	External interrupt polarity control register

Interrupt SFR list

7.3.1. Interrupt SFR Detailed Description

INT_PE_STAT(85H)WDT/Timer2 interrupt status register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	-	INT_WDT_STAT	INT_TIMER2_STAT
R/W	-	-	-	-	-	-	R/W	R/W
Reset value	-	-	-	-	-	-	0	0

Bit number	Bit symbol	Description
1	INT_WDT_STAT	WDT interrupt status, set 0, write WDT_CTRL can set 0. 1: interrupt effective 0: invalid interrupt
0	INT_TIMER2_STAT	TIMER2 interrupt status, set 0, write TIMER2_CFG can set 0. 1: interrupt effective 0: invalid interrupt

INT_POBO_STAT (86H) LVDT boost/LVDT buck interrupt status register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	-	INT_PO_STAT	INT_BO_STAT
R/W	-	-	-	-	-	-	R/W	R/W
Reset value	-	-	-	-	-	-	0	0

Bit number	Bit symbol	Description
1	INT_PO_STAT	Lvdt boost interrupt status 1: boost interrupt is valid 0: boost interrupt is invaild
0	INT_BO_STAT	Lvdt buck interrupt state 1: buck interrupt is valid 0: buck interrupt is invalid

TCON(88H) Timer control register

Bit number	7	6	5	4	3	2	1	0
Symbol	TF1	TR1	TF0	TR0	IE1	-	IE0	-
R/W	R/W	R/W	R/W	R/W	R/W	-	R/W	-
Reset value	0	0	0	0	0	-	0	-

Bit number	Bit symbol	Description
3	IE1	External interrupt 1. The hardware set 1, the software is cleared.
1	IE0	External interrupt 0. The hardware set 1, the software is cleared

IEN0(A8H) Interrupt enable register

Bit number	7	6	5	4	3	2	1	0
Symbol	EA	-	-	-	ET1	EX1	ET0	EX0
R/W	R/W	-	-	-	R/W	R/W	R/W	R/W
Reset value	0	-	-	-	0	0	0	0

Bit number	Bit symbol	Description
7	EA	Interrupt enable bit 0: Mask all interrupts (EA has priority over the respective interrupt enable bits of the interrupt sources); 1: The interrupt is turned on. Whether the interrupt request of each interrupt source is allowed or forbidden is determined by the respective enable bit.
6~4	--	Reserved
3	ET1	Timer1 interrupt enable bit 0: Disable timer 1 to apply for interrupt; 1: Allow timer 1 flag bit to apply for interrupt.
2	EX1	INT_EXT1 enable bit 0: Disable INT_EXT1 to apply for interrupt; 1: Allow INT_EXT1 to apply for interrupt.
1	ET0	Timer 0 interrupt enable bit 0: Disable timer 0 (TF0) to apply for interrupt; 1: Allow TF0 flag bit to request interrupt.
0	EX0	INT_EXT0 enable bit 0: Disable INT_EXT0 to apply for interrupt; 1: Allow INT_EXT0 to apply for interrupt.

IPL0 (B8H) Interrupt priority register 0

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	PT1	PX2	PT0	PX0
R/W	-	-	-	-	R/W	R/W	R/W	R/W
Reset value	-	-	-	-	0	0	0	0

Bit number	Bit symbol	Description
7~4	-	Reserved
3	PT1	TF1(Timer1 interrupt) priority selection bit. 0: TF1(Timer1 interrupt) is low priority. 1: TF1(Timer1 interrupt) is high priority.
2	PX2	INT_EXT1 interrupt priority selection bit. 0: INT_EXT1 is low priority. 1: INT_EXT1 is high priority.
1	PT0	TF0(Timer0 interrupt) priority selection bit. 0: TF0(Timer0 interrupt) is low priority. 1: TF0(Timer0 interrupt) is high priority.
0	PX0	INT_EXT0 interrupt priority selection bit. 0: INT_EXT0 is low priority. 1: INT_EXT0 is high priority.

PERIPH_IO_SEL3(ACH) INT3 select enable register 3

Bit number	7	6	5	4
Symbol	-	INT3_22_IO_SEL	INT3_21_IO_SEL	INT3_20_IO_SEL
R/W	-	R/W	R/W	R/W
Reset value	-	0	0	0
Bit number	3	2	1	0
Symbol	INT3_19_IO_SEL	INT3_18_IO_SEL	INT3_17_IO_SEL	INT3_16_IO_SEL
R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0

Bit number	Bit symbol	Description
6~0	INT3_n_IO_SEL (n=22~16)	INT3_n port selection enable 1: Select INT function; 0: INT function is not selected

PERIPH_IO_SEL2(ADH) INT3 select enable register 2

Bit number	7	6	5	4
Symbol	INT3_15_IO_SEL	INT3_14_IO_SEL	INT3_13_IO_SEL	INT3_12_IO_SEL
R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0
Bit number	3	2	1	0
Symbol	INT3_11_IO_SEL	INT3_10_IO_SEL	INT3_9_IO_SEL	INT3_8_IO_SEL
R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0

Bit number	Bit symbol	Description
7~0	INT3_n_IO_SEL (n=15~8)	INT3_n port selection enable 1: Select INT function; 0: INT function is not selected

PERIPH_IO_SEL1(AEH) INT3 select enable register 1

Bit number	7	6	5	4
Symbol	INT3_7_IO_SEL	INT3_6_IO_SEL	INT3_5_IO_SEL	INT3_4_IO_SEL
R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0
Bit number	3	2	1	0
Symbol	INT3_3_IO_SEL	INT3_IO_2_SEL	INT3_1_IO_SEL	INT3_0_IO_SEL
R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0

Bit number	Bit symbol	Description

7~0	INT3_n_IO_SEL (n=7~0)	INT3_n port selection enable 1: Select INT function; 0: INT function is not selected

IRCON2 (E1H) Interrupt flag register 2

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	IE11	IE10	IE9	IE8
R/W	-	-	-	-	R/W	R/W	R/W	R/W
Reset value	-	-	-	-	0	0	0	0

Bit number	Bit symbol	Description
7~4	--	Reserved
3	IE11	External interrupt 3 interrupt flag 1: There is a INT3 interrupt flag; 0: No INT3 interrupt flag
2	IE10	UART1 interrupt flag 1: There is a UART1 interrupt flag; 0: No UART1 interrupt flag
1	IE9	UART0 interrupt flag 1: There is a UART0 interrupt flag; 0: No UART0 interrupt flag
0	IE8	LVDT interrupt flag 1: There is a LVDT interrupt flag; 0: No LVDT interrupt flag

IEN1 (E6H) Interrupt enable register 1

Bit number	7	6	5	4	3	2	1	0
Symbol	EX7	EX6	EX5	EX4	EX3	EX2	-	-
R/W	R/W	R/W	R/W	R/W	R/W	R/W	-	-
Reset value	0	0	0	0	0	0	-	-

Bit number	Bit symbol	Description
7	EX7	WDT/Timer2 interrupt enable 1: interrupt enable; 0: interrupt disable
6	EX6	LED interrupt enable 1: interrupt enable; 0: interrupt disable
5	EX5	CSD interrupt enable 1: interrupt enable; 0: interrupt disable
4	EX4	ADC interrupt enable 1: interrupt enable; 0: interrupt disable
3	EX3	IIC interrupt enable 1: interrupt enable; 0: interrupt disable

2	EX2	External interrupt 2 interrupt enable 1: interrupt enable; 0: interrupt disable
1~0	-	Reserved

IEN2(E7H) Interrupt enable register 2

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	EX11	EX10	EX9	EX8
R/W	-	-	-	-	R/W	R/W	R/W	R/W
Reset value	-	-	-	-	0	0	0	0

Bit number	Bit symbol	Description
7~4	-	Reserved
3	EX11	External interrupt 3 interrupt enable 1: interrupt enable; 0: interrupt disable
2	EX10	UART1 interrupt enable 1: interrupt enable; 0: interrupt disable
1	EX9	UART0 interrupt enable 1: interrupt enable; 0: interrupt disable
0	EX8	LVDT interrupt enable 1: interrupt enable; 0: interrupt disable

IRCON1 (F1H) Interrupt flag register 1

Bit number	7	6	5	4	3	2	1	0
Symbol	IE7	IE6	IE5	IE4	IE3	IE2	-	-
R/W	R/W	R/W	R/W	R/W	R/W	R/W	-	-
Reset value	0	0	0	0	0	0	-	-

Bit number	Bit symbol	Description
7	IE7	WDT/Timer2 interrupt flag 1: There is a WDT/Timer2 interrupt flag; 0: No WDT/Timer2 interrupt flag
6	IE6	LED interrupt flag 1: There is a LED interrupt flag; 0: No LED interrupt flag
5	IE5	CSD interrupt flag 1: There is a CSD interrupt flag; 0: No CSD interrupt flag
4	IE4	ADC interrupt flag 1: There is a ADC interrupt flag;

		0: No ADC interrupt flag
3	IE3	IIC interrupt flag 1: There is a IIC interrupt flag; 0: No IIC interrupt flag
2	IE2	External interrupt 2 interrupt flag 1: There is a INT2 interrupt flag; 0: No INT2 interrupt flag
1~0	-	Reserved

PERIPH_IO_SEL (F2H) IIC /INT function control register

Bit number	7	6	5	4	3
Symbol	-	IIC_AFIL_SEL	IIC_DFIL_SEL	IIC_IO_SEL	
R/W	-	R/W	R/W	R/W	R/W
Reset value	-	1	0	0	0
Bit number	2	1	0	/	
Symbol	INT2_IO_SEL	INT1_IO_SEL	INT0_IO_SEL	/	
R/W	R/W	R/W	R/W		
Reset value	0	0	0		

Bit number	Bit symbol	Description
2	INT2_IO_SEL	INT2 select enable, correspond PD7 1: select INT2 function 0: not select INT2 function
1	INT1_IO_SEL	INT1 select enable, correspond PD6 1: select INT1 function 0: not select INT1 function
0	INT0_IO_SEL	INT0 select enable, correspond PD0 1: select INT0 function 0: not select INT0 function

IPL2 (F4H) Interrupt priority register 2

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	IPL2.3	IPL2.2	IPL2.1	IPL2.0
R/W	-	-	-	-	R/W	R/W	R/W	R/W
Reset value	-	-	-	-	0	0	0	0

Bit number	Bit symbol	Description
7~4	--	Reserved
3	IPL2.3	External interrupt 3 interrupt priority 0: low priority; 1: high priority
2	IPL2.2	UART1 interrupt priority. 0: low priority; 1: high priority

1	IPL2.1	UART0 interrupt priority. 0: low priority; 1: high priority
0	IPL2.0	LVDT interrupt priority. 0: low priority; 1: high priority

IPL1 (F6H) Interrupt priority register 1

Bit number	7	6	5	4	3	2	1	0
Symbol	IPL1.7	IPL1.6	IPL1.5	IPL1.4	IPL1.3	IPL1.2	-	-
R/W	R/W	R/W	R/W	R/W	R/W	R/W	-	-
Reset value	0	0	0	0	0	0	-	-

Bit number	Bit symbol	Description
7	IPL1.7	WDT/Timer 2 interrupt priority. 0: low priority; 1: high priority
6	IPL1.6	LED interrupt priority. 0: low priority; 1: high priority
5	IPL1.5	CSD interrupt priority. 0: low priority; 1: high priority
4	IPL1.4	ADC interrupt priority. 0: low priority; 1: high priority
3	IPL1.3	IIC interrupt priority. 0: low priority; 1: high priority
2	IPL1.2	External interrupt 2 priority. 0: low priority; 1: high priority
1~0	--	Reserved

EXT_INT_CON (F7H) External interrupt polarity control register

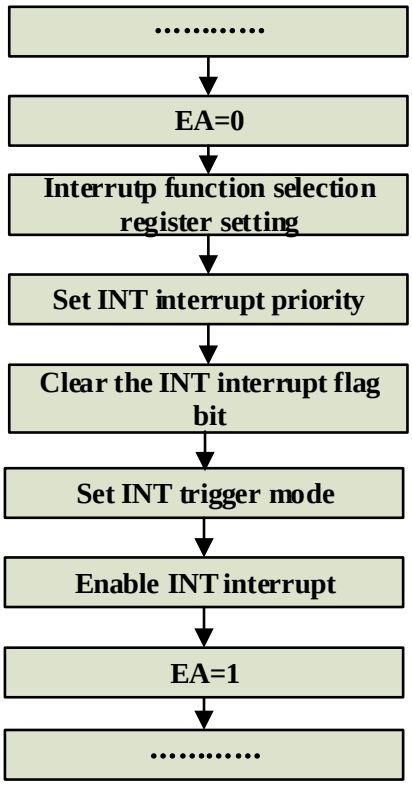
Bit number	7	6	5	4
Symbol	-	INT3_POLARITY	INT2_POLARITY	
R/W	-	R/W	R/W	R/W
Reset value	-	0	0	1
Bit number	3	2	1	0
Symbol	INT1_POLARITY		INT0_POLARITY	
R/W	R/W	R/W	R/W	R/W
Reset value	0	1	0	1

Bit number	Bit symbol	Description
6	INT3_POLARITY	External interrupt 3_x trigger polarity selection: 1: Rising edge (high level wake-up in idle mode 1) 0: Falling edge (low-level wake-up in idle mode 1)
5~4	INT2_POLARITY	External interrupt 2 trigger polarity selection:

		01: Falling edge (low-level wake-up in idle mode 1) 10: rising edge (high level wake-up in idle mode 1) 00/11: Double edge (low-level wake-up in idle mode 1)
3~2	INT1_POLARITY	External interrupt 1 trigger polarity selection: 01: Falling edge (low-level wake-up in idle mode 1) 10: rising edge (high level wake-up in idle mode 1) 00/11: Double edge (low-level wake-up in idle mode 1)
1~0	INT0_POLARITY	External interrupt 0 trigger polarity selection: 01: Falling edge (low-level wake-up in idle mode 1) 10: rising edge (high level wake-up in idle mode 1) 00/11: Double edge (low-level wake-up in idle mode 1)

Note: INT3 shares an interrupt vector and can only respond to one external interrupt at the same time. When the multi-channel pin external interrupt rising edge or falling edge trigger is enabled, all the enabled external interrupt pins must be released during the detection process to respond to the current trigger signal (when the falling edge is triggered, the release is high. When the rising edge is triggered, the release is low).

7.4. External Interrupt Configuration Process



INT0/1/2/3 configuration process chart

8. Timer

The BF7812AMXX-XJLX contains three Timers (Timer0/Timer1/Timer2). Each Timer contains a 16-bit register that appears as two bytes when accessed: a low byte (TL0 or TL1) and a high byte (TH0 or TH1). Timer2 register is low byte TIMER2_SET_L, high byte TIMER2_SET_H.

Timer features:

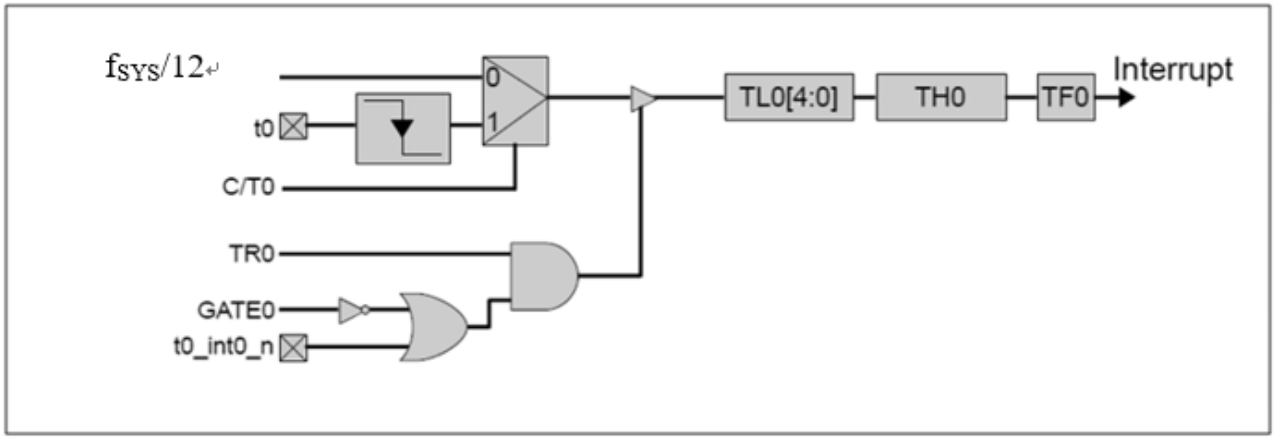
- 3*16-bit Timers
- Timer0 clock source: f_{SYS}, the internal frequency of the timer clock is f_{SYS} 1/12;
- Timer1 clock source: f_{SYS}, the internal frequency of the timer clock is f_{SYS} 1/12;
- Timer2 clock source is LIRC or XTAL 32768Hz/4MHz
- Timer0 support 8bits automatic reload timing/counting, 16bits manual reload timing/counting function;
- Timer1 support 8bits automatic reload timing/counting, 16bits manual reload timing/counting function;
- Timer2 support 16bits automatic reload timing and manual reload timing, support interrupt wake-up function.

8.1. Timer0 and Timer1

The Timer 0/1 has four operating modes, controlled by TMOD SFR and TCON SFR.
Timer0/1 four modes of operation as follows:

- 13 bit timer (mode 0)
- 16 bit timer (mode 1)
- Automatic overload 8-bit timer (mode 2)
- Two 8-bit timer (Mode 3)

Mode 0：13 bit timer

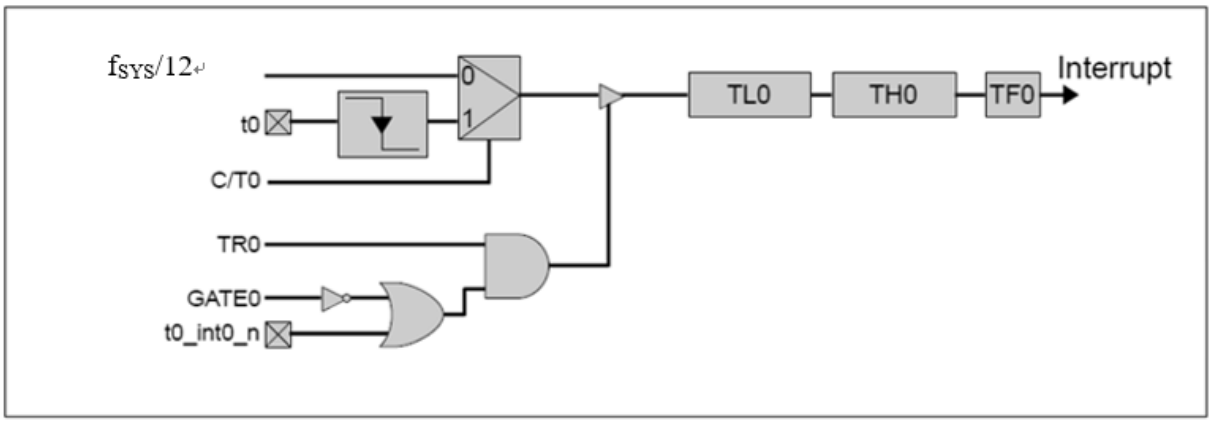


Mode 0 logical structure diagram

In mode 0, timer 0 and timer 1 work the same process, at the picture shows. In mode 0, Timer is 13bit counter, bit0-4 are TL0 (or TL1), the other 8 bits are TH0 (or TH1). In TCON register (TR0/TR1) to control timer0/1 start or stop.

The Timer counts the selected clock source(f_{SYS} /12); When the 13bit counter counts up to all 1, the counter is cleared to 0(all 0) and TF0(or TF1)is set. In mode 0, TL0 (or TL1) high 3bit is not sure. These 3bit should be masked or ignored when reading the count value. t0/t1, C/T0/CT1 all 0, t0_int0_n/t1_int1_n all 1, count enable is only TR0/1.

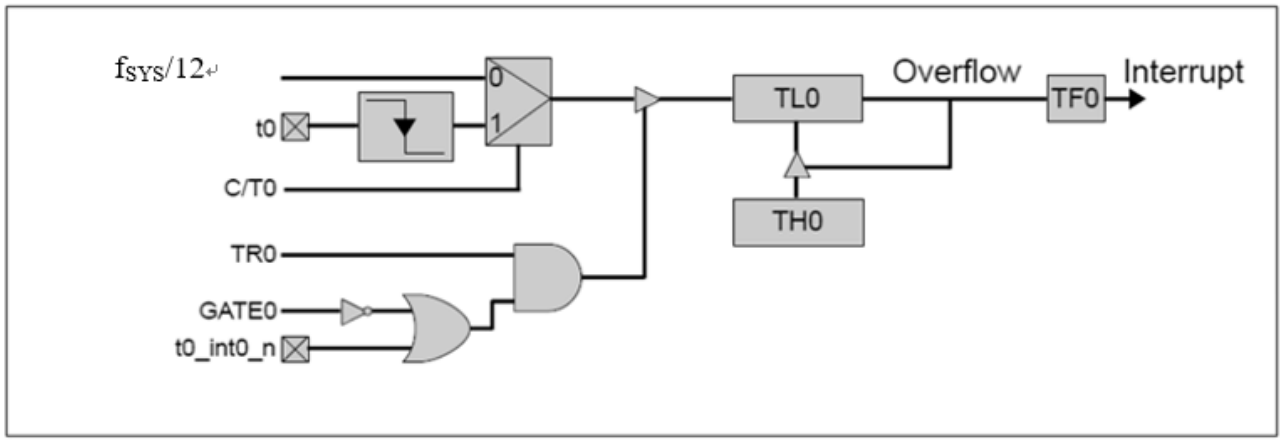
Mode 1: 16 bit timer



Mode 1 logical structure diagram

In mode 1, timer 0 and timer 1 work the same process. At the picture shows, in mode 1, Timer is 16bit counter, all 8 bits of the LSB register (TL0 or TL1) are used. When the counter count is accumulated to 0xFFFF, the counter is cleared to 0. In addition, mode 1 and mode 2 are the same. t0/t1, C/T0/CT1 all 0, t0_int0_n/t1_int1_n all 1, count enable is only determined by TR0/1.

Mode2: reload initial value 8bit timer

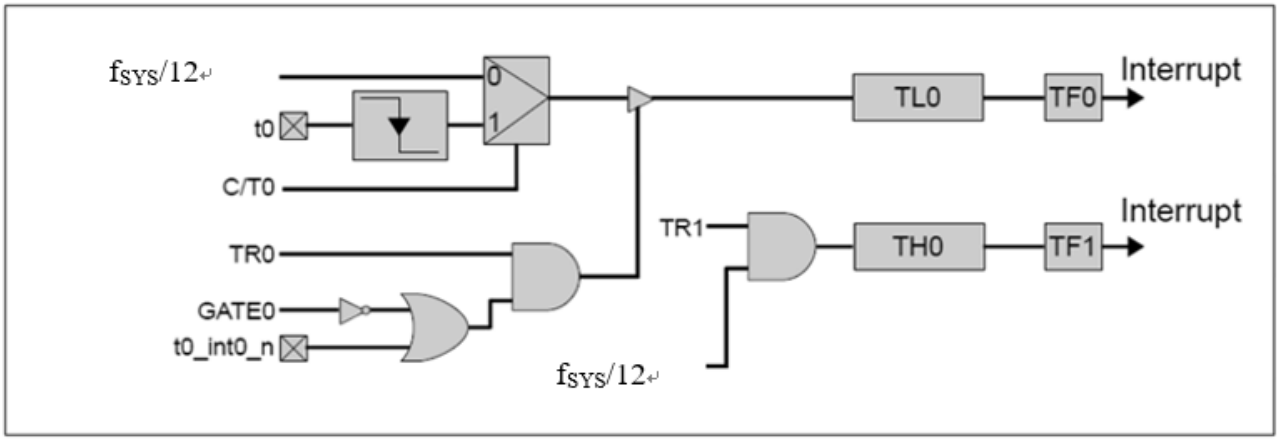


Mode 2 logical structure diagram

The modes of Timer0 and Timer1 are the same. In mode 2, the Timer is an 8bit timer with an automatic reload initial value. This counter is the LSB register (TL0 or TL1). The initial value that needs to be reloaded is saved in the MSB register (TL0 or TL1).

At the picture shows, mode 2 counter control is the same as mode 0 and mode 1. But in mode 2, When the TLn count is accumulated to FFh, the value stored in THn is overloaded to TLn. t0/t1, C/T0/CT1 all 0, t0_int0_n/t1_int1_n all 1, count enable is only determined by TR0/1.

Mode3: Two 8bit timer



Mode 3 logical structure diagram

In mode3, timer0 is two 8bit timer, then timer 1 stop count and save the value. Show as below, TL0 is an 8-bit register controlled by the control bit of Timer0. The counter uses GATE as the enable terminal to control the INT_EXT signal reception.

TH0 is a separate 8-bit counter. TH0 only used to count the clock cycle (f_{SYS}/12). Timer1 control bit and flag bit (TR1 and TF1) used as the TH0's control bit and flag.

When timer0 working in mode3, the use of Timer 1 is limited because Timer 0 uses the Timer 1 control(TR1) and interrupt flags(TF1). Timer 1 can still be used to generate baud rate. The value of TL1 and TH1 is still effective.

When timer0 working in mode 3, though mode control bit of Timer1 to control Timer1. In order to start timer1, need to set Timer 1 to mode 0, 1 or 2. Configure timer1 working in mode3, make timer1 stop. Timer 1 can be used as a Timer (clock is clk/12), However, since TR1 and TF1 are borrowed, overflow interrupts cannot be generated. When timer0 working in mode 3, timer1's GATE is effective. t0/t1, C/T0/CT1 all 0, t0_int0_n/t1_int1_n all 1, count enable is only determined by TR0/1.

8.1.1. Timer0/1 Related Register

SFR register				
Address	**Name**	**RW**	**Reset value**	**Function description**
0x88	TCON	RW	xx00_xx00b	Timer control register
0x89	TMOD	RW	0000_0000b	Timer mode register
0x8A	TL0	RW	0000_0000b	Timer 0 counter low 8 bits
0x8B	TL1	RW	0000_0000b	Timer 1 counter low 8 bits
0x8C	TH0	RW	0000_0000b	Timer 0 counter high 8 bits
0x8D	TH1	RW	xx00_xx00b	Timer 1 counter high 8 bits
0xA8	IEN0	RW	0xxx_0000b	Interrupt enable register
0xB8	IPL0	RW	xxxx_0000b	Interrupt priority register 0

Timer0/1 SFR list

8.1.2. Timer0/1 Register Detailed Description

TCON(88H) Timer control register

Bit number	7	6	5	4	3	2	1	0
Symbol	TF1	TR1	TF0	TR0	IE1	-	IE0	-
R/W	R/W	R/W	R/W	R/W	R/W	-	R/W	-
Reset value	0	0	0	0	0	-	0	-

Bit number	Bit symbol	Description
7	TF1	Timer1 overflow flag. Set to 1 when Timer1 overflows, or Timer0's TH0 overflows in mode three.
6	TR1	Timer1 start enable.When set to 1, enable the Timer1 count or Timer0 TH0 count in mode 3.
5	TF0	Timer0 overflow flag. The hardware set 1 when Timer0 overflows.
4	TR0	Timer0 start enable, when set to 1, start Timer0 count.

TMOD(89H) Timer mode register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	M1[1:0]		-	-	M0[1:0]	
R/W	-	-	R/W		-	-	R/W	
Reset value	-	-	0	0	-	-	0	0

Bit number	Bit symbol	Description
7~6, 3~2	--	Reserved
5~4	M1[1:0]	Timer1 mode select bits 00=mode0 – 13 bit timer 01=mode1 – 16 bit timer 10=mode2 – automatic reload mode 8bit timer 11=mode3 – 2*8bit timer
1~0	M0[1:0]	Timer0 mode select bits 00=mode0 – 13 bit timer 01=mode1 – 16 bit timer 10=mode2 – automatic reload mode 8bit timer 11=mode3 – 2*8bit timer

TL0(8AH) Timer 0 counter low 8 bits

Bit number	7	6	5	4	3	2	1	0
Symbol	TL0[7:0]							
R/W	R/W							
Reset value	0							

TL1(8BH) Timer 1 counter 8 bits

Bit number	7	6	5	4	3	2	1	0
Symbol	TL1[7:0]							
R/W	R/W							
Reset value	0							

TH0(8CH) Timer 0 counter high 8 bits

Bit number	7	6	5	4	3	2	1	0
Symbol	TH0[7:0]							
R/W	R/W							
Reset value	0							

TH1(8DH) Timer 1 counter high 8 bits

Bit number	7	6	5	4	3	2	1	0
Symbol	TH1[7:0]							
R/W	R/W							
Reset value	0							

IEN0(A8H) Interrupt enable register

Bit number	7	6	5	4	3	2	1	0
Symbol	EA	-	-	-	ET1	EX1	ET0	EX0
R/W	R/W	-	-	-	R/W	R/W	R/W	R/W
Reset value	0	-	-	-	0	0	0	0

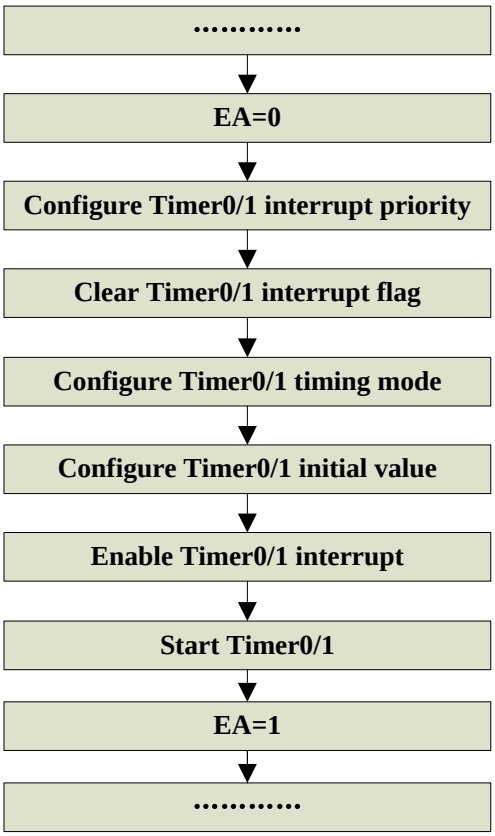
Bit number	Bit symbol	Description
7	EA	Interrupt enable bit 0: Mask all interrupts (EA has priority over the respective interrupt enable bits of the interrupt sources); 1: The interrupt is turned on. Whether the interrupt request of each interrupt source is allowed or forbidden is determined by the respective enable bit.
3	ET1	Timer1 interrupt enable bit 0: Disable timer 1 to apply for interrupt; 1: Allow timer 1 flag bit to apply for interrupt.
1	ET0	Timer 0 interrupt enable bit 0: Disable timer 0 (TF0) to apply for interrupt; 1: Allow TF0 flag bit to request interrupt.

IPL0 (B8H) Interrupt priority register 0

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	PT1	PX2	PT0	PX0
R/W	-	-	-	-	R/W	R/W	R/W	R/W
Reset value	-	-	-	-	0	0	0	0

Bit number	Bit symbol	Description
3	PT1	TF1(Timer1 interrupt) priority selection bit. 0: TF1(Timer1 interrupt) is low priority. 1: TF1(Timer1 interrupt) is high priority.
1	PT0	TF0(Timer0 interrupt) priority selection bit. 0: TF0(Timer0 interrupt) is low priority. 1: TF0(Timer0 interrupt) is high priority.

8.1.3. Timer0/1 Configure Process



Timer0/1 configure process

8.2. Timer2

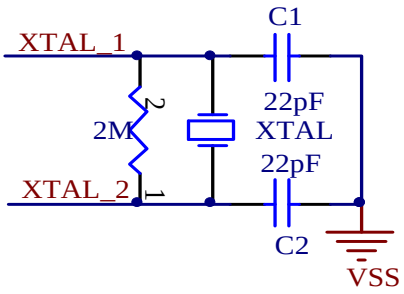
Timer2 module plays a timing role, the internal structure of the Timer2 module is a 16-bit counter. Timed function by counting the input clock, the counting principle of Timer2 is the accumulation counts to the set value. Timer2's count clock can be selected from the external XTAL clock and LIRC. Timer2 has two working modes: signal time mode and automatic reload mode, regardless of the mode, the timing is completed and an interruption occurs.

TIMER2_EN configuration Timer2 function enable, TIMER2_RLD configuration automatic reload mode and manual reload mode. Timing time is determined by registers TIMER2_SET_L and TIMER2_SET_H. The time clock can choose LIRC and XTAL 32768Hz/4MHz, which is determined by the clock selection register. Timer2 support interrupt wake up in idle mode 1, software clear interrupt flag is required in the interrupt handler.

Timer2 timing duration formula:

$T_{TIMER2}=65536*T_{TIMER2\_CLK}*(\{TIMER2\_SET\_H, TIMER2\_SET\_L\}+1)$

Note: T_{TIMER2_CLK} = 1/32768 (s) orT_{TIMER2_CLK} = 1/4M (s)



External crystal oscillator circuit reference

Notes:

1. **Arbitrary configuration TIMER2_SET_H, TIMER2_SET_L, TIMER2_CFG will clear counter;**
2. **External crystal oscillator circuit is for reference only, actual reference cryatal specifications.**

8.2.1. Timer2 Related Register

SFR register				
Address	**Name**	**RW**	**Reset value**	**Function description**
0x85	INT_PE_STAT	RW	xxxx_xx00b	WDT/Timer2 interrupt status register
0x93	TIMER2_CFG	RW	xxxx_x000b	TIMER2 configuration register
0x94	TIMER2_SET_H	RW	0000_0000b	TIMER2 counter configuration register, high 8 bits
0x95	TIMER2_SET_L	RW	0000_0000b	TIMER2 counter configuration register, low 8 bits
0xE6	IEN1	RW	0000_00xxb	Interrupt enable register 1
0xF1	IRCON1	RW	0000_00xxb	Interrupt flag register 1
0xF6	IPL1	RW	0000_00xxb	Interrupt priority register 1
0xFE	PD_ANA	RW	xx00_0111b	Module switch control register

Timer2 registers list

8.2.2. Timer2 Register Detailed Description

INT_PE_STAT(85H)WDT/Timer2 interrupt status register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	-	INT_WDT_STAT	INT_TIMER2_STAT
R/W	-	-	-	-	-	-	R/W	R/W
Reset value	-	-	-	-	-	-	0	0

Bit number	Bit symbol	Description
0	INT_TIMER2_STAT	TIMER2 interrupt status, set 0, write TIMER2_CFG can set 0. 1: interrupt effective 0: invalid interrupt

TIMER2_CFG (93H) TIMER2 CFG register

Bit number	7~3	2	1	0
Symbol	-	TIMER2_CLK_SEL	TIMER2_RLD	TIMER2_EN
R/W	-	R/W	R/W	R/W
Reset value	-	0	0	0

Bit number	Bit symbol	Description
7~3	--	reserved
2	TIMER2_CLK_SEL	TIMER2 clock select register 1: select XTAL 32768Hz/4MHz 0: select LIRC

1	TIMER2_RLD	TIMER2 reload enable control register 1: automatic reload mode 0: manual reload mode
0	TIMER2_EN	TIMER2 count enable register 1: turn on timing; 0: stop timing; In manual reload mode, the hardware automatically clears this register after timing is completed, stop count. In manual reload mode, will maintain the enable register after the count is completed. Automatically re-counting from 0, no matter which mode, configuring this register to 1 during counting will start counting from 0.

TIMER2_SET_H(94H) TIMER2 count value configuration register, high 8 bits

Bit number	7	6	5	4	3	2	1	0
Symbol	-							
R/W	R/W							
Reset value	0							

Bit number	Bit symbol	Description
7~0	--	TIMER2 count configuration register, high 8 bits. Configuring this register during the scan will recount.

TIMER2_SET_L(95H) TIMER2 count value configuration register, low 8 bits

Bit number	7	6	5	4	3	2	1	0
Symbol	-							
R/W	R/W							
Reset value	0							

Bit number	Bit symbol	Description
7~0	--	TIMER2 count configuration register, low 8 bits. Configuring this register during the scan will recount.

IEN1 (E6H) Interrupt enable register 1

Bit number	7	6	5	4	3	2	1	0
Symbol	EX7	EX6	EX5	EX4	EX3	EX2	-	-
R/W	R/W	R/W	R/W	R/W	R/W	R/W	-	-
Reset value	0	0	0	0	0	0	-	-

Bit number	Bit symbol	Description
7	EX7	WDT/Timer2 interrupt enable 1: interrupt enable; 0: interrupt disable

IRCON1 (F1H) Interrupt flag register 1

Bit number	7	6	5	4	3	2	1	0
Symbol	IE7	IE6	IE5	IE4	IE3	IE2	-	-
R/W	R/W	R/W	R/W	R/W	R/W	R/W	-	-
Reset value	0	0	0	0	0	0	-	-

Bit number	Bit symbol	Description
7	IE7	WDT/Timer2 interrupt flag 1: There is a WDT/Timer2 interrupt flag; 0: No WDT/Timer2 interrupt flag

IPL1 (F6H) Interrupt priority register 1

Bit number	7	6	5	4	3	2	1	0
Symbol	IPL1.7	IPL1.6	IPL1.5	IPL1.4	IPL1.3	IPL1.2	-	-
R/W	R/W	R/W	R/W	R/W	R/W	R/W	-	-
Reset value	0	0	0	0	0	0	-	-

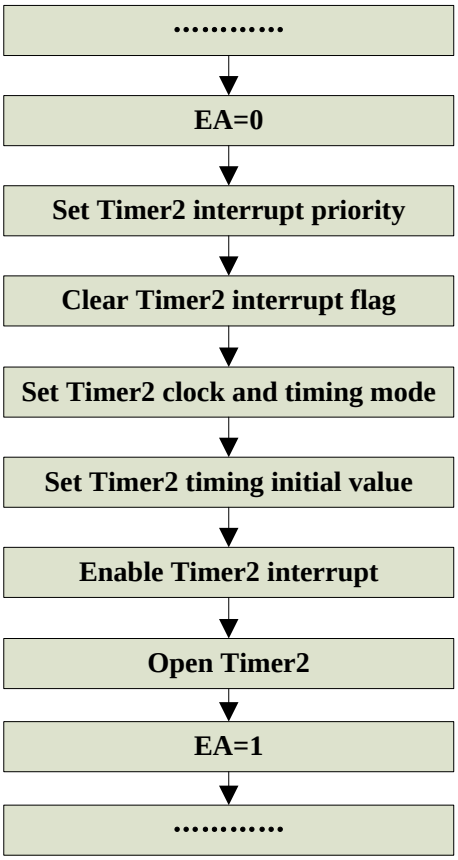
Bit number	Bit symbol	Description
7	IPL1.7	WDT/Timer 2 interrupt priority. 0: low priority; 1: high priority

PD_ANA (FEH) Module switch control register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	LDO_ LOAD2	LDO_ LOAD1	XTAL_SEL	PD_XTAL	PD_CSD	PD_ADC
R/W	-	-	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	-	-	0	0	0	1	1	1

Bit number	Bit symbol	Description
7~6	-	Reserved
3	XTAL_SEL	RTC crystal oscillator circuit control register 1: Select 4MHz; 0: Select 32768Hz
2	PD_XTAL	RTC crystal oscillator circuit control register. 1: close; 0: open; default close.

8.2.3. Timer2 Configure Process



Timer2 configure process table

In the configuration process:

1. First configure the timing set value register TIMER2_SET_H/TIMER2_SET_L and step configuration TIMER2_CNT_MOD;
2. Then automatically reload the enable register TIMER2_RLD according to the configuration, set to 1 if automatic loop count is required, otherwise configure 0;
3. Final configuration timing enable register TIMER2_EN, enable timing configuration TIMER2_EN=1;
4. Stop timing: TIMER2_EN=0.

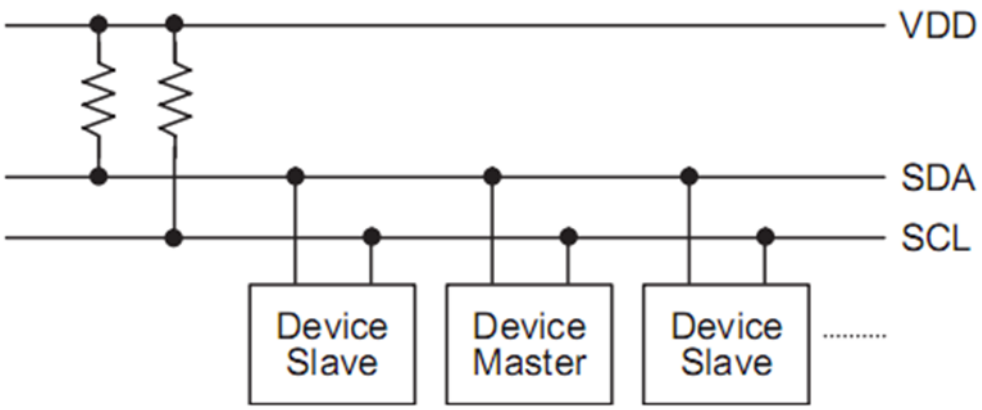
Notes:

1. **TIMER2_EN=0x1 to be placed at the end of all configurations;**
2. **During the TIMER2 timing, it is forbidden to change the configuration of Timer2. To modify, you need to stop timing first;**
3. **For precise timing, in the auto-reload mode, it is not allowed to configure three registers of TIMER2 in interrupt processing.**

9. IIC

The BF7812AMXX-XJLX supports standard and fast IIC communication, and has the following characteristics:

- Two serial interfaces: serial data line SDA and serial clock line SCL;
- Meet philips's standard communication protocol;
- Transmission rate: 100 kHz, 400 kHz;
- Support for 7-bit address addressing;
- Has the function of extending the clock low level;
- In idle mode 1, wake up the core through the IIC interrupt;
- Detect write conflicts and cache BUF overflow exceptions;
- Support digital filter function and analog filter function of IIC port.



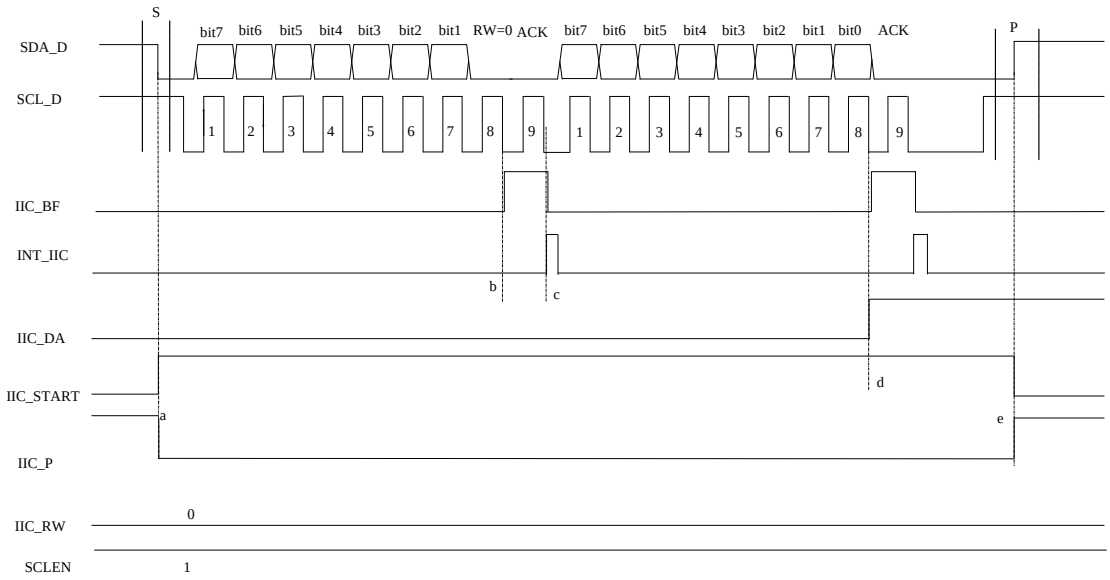
IIC master-slave

The master and slave from the SCL (serial clock) line, SDA (serial data) wire connection, in the communication mode, the PA0/PA1/PD6 is open drain, SCL, SDA must be connected to the pull resistor(suggest 4.7K~10K). When the TS device has touch related actions, such as touch, slide, figure away, etc. The master can read the state of the slave through IIC communication.

9.1. Communication Timing

The BF7812AMXX-XJLX uses hardware slave. When the host reads/writes data, after the slave receives the address, if the address matches, an interrupt is generated and a valid response signal is sent. And an interrupt is generated after the host computer writes the eighth clock of the data, and the host will not generate an interrupt signal when sending the stop signal. IIC timing diagram as follows:

IIC host write timing diagram



IIC write not pull down clock line diagram

As shown in the above figure, the schematic diagram of the clock line is not pulled down during the host write operation. From this, you can see the changes of the IIC bus and some internal signal changes.

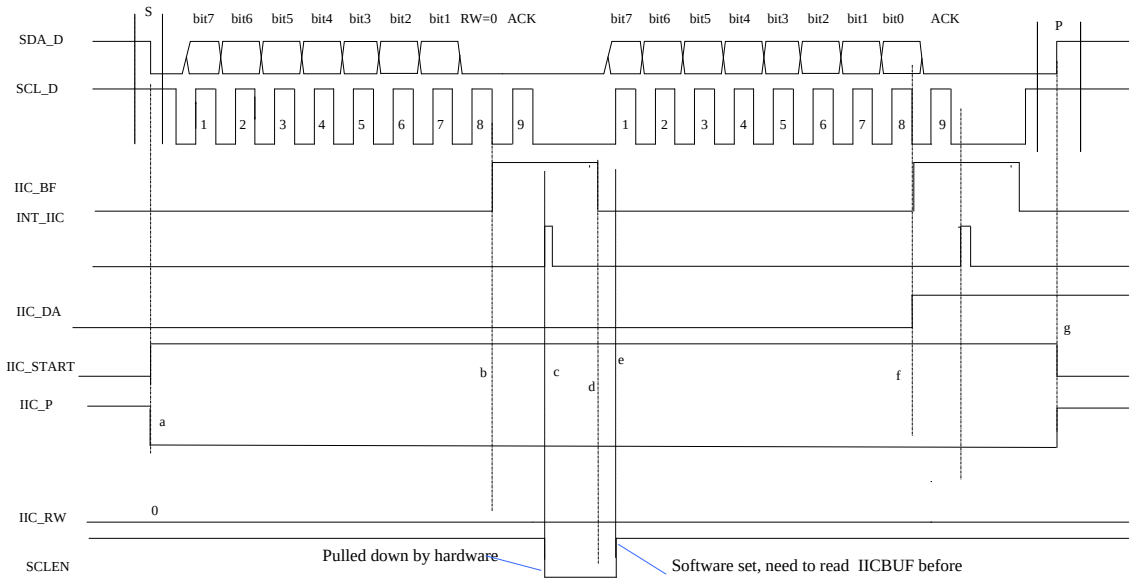
First the host sends a start signal IIC_START, and the slave sets the IIC_START status bit after detecting the IIC_START signal, as shown by the dotted line a in the figure.

Then the host sends the address bytes and write flag bit, and the slave automatically compares with its own address after receiving the address byte. Set IIC_BF after the falling edge of the eighth clock if the address matches, as shown by the dotted line b in the figure. An interrupt signal INT_IIC is generated after the falling edge of the ninth clock, as shown by the dotted line c. The MCU executes interrupt subroutine device needs to read IICBUF. Even if this data is not useful, it needs to be operated.Reading the IICBUF operation will indirectly clear the START_BF. The host continues to send messages. The IIC_BF is also set after the falling edge of the 8th clock of the 2nd byte, and the IIC_AD flag is also set. The currently received byte of the flag is data, and the stop signal has no effect on the IIC_STOP flag. That is, the stop signal IIC_STOP is detected, as shown by the dotted line d. And the IIC_AD flag will not be cleared. The interrupt is generated after the

falling edge of the ninth clock, and the interrupt subroutine requires the same operation. If the host wants to send multiple bytes, it can continue to send. The figure above only shows the case where the host sends a data.

Finally, the host sends a stop signal IIC_STOP after sending all the data, indicating the end of the communication, releasing the IIC bus, and the bus enters the idle state.

IIC host write pull low timing diagram



IIC write low clock line diagram

As shown in the above figure, it is a schematic diagram of pulling down the clock line during the host write operation, from which you can see the changes of the IIC bus and some internal signal changes.

First the host sends a start signal IIC_START, and the slave sets the IIC_START status bit after detecting the IIC_START signal, as shown by the dotted line a.

Then the host sends the address bytes and write flag bit, and the slave automatically compares with its own address after receiving the address byte. Set IIC_BF after the falling edge of the eighth clock if the address matches, as shown by the dotted line b.

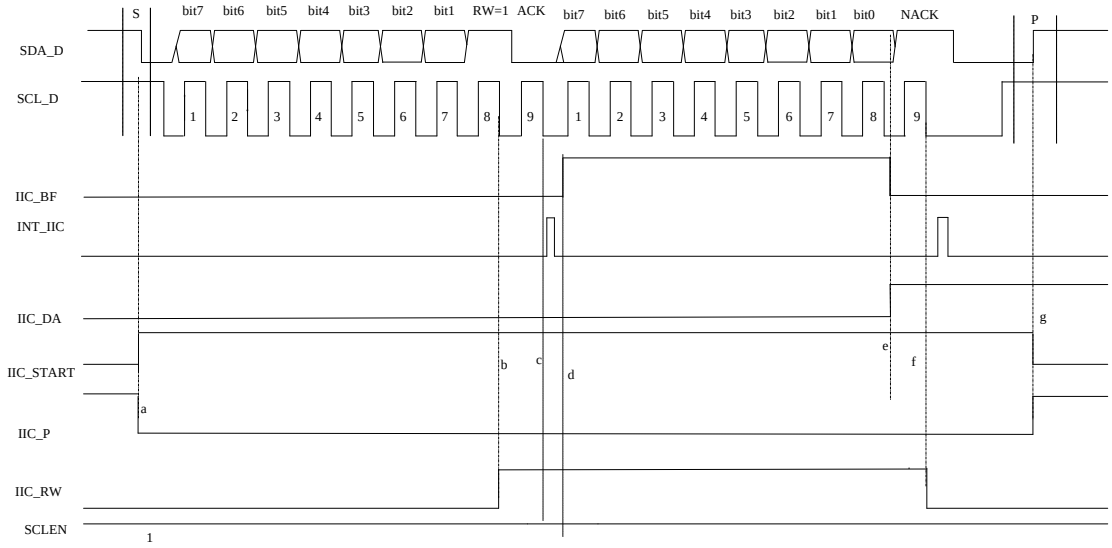
An interrupt signal INT_IIC is generated after the falling edge of the ninth clock, as shown by the dotted line c. SCLEN will be cleared by hardware. This process is used to process or read data from the slave. Even if this data is not useful, reading IICBUF will cause IIC_BUF to be cleared indirectly, as shown by the dotted line d. Software sets SCLEN to release the clock line.As shown by the dotted line e.

After the master detects that the slave releases the SCL, it continues to send the synchronous clock. The IIC_BF is also set after the falling edge of the 8th clock of the 2nd byte, and the IIC_AD flag is also set. And the IIC_AD flag is also set. The currently received byte of the flag is data, as shown by the dotted line f, and the stop signal has no effect on the IIC_STOP flag. That is, the stop signal IIC_STOP is detected, and the IIC_AD flag will not be cleared; The interrupt is generated

after the falling edge of the ninth clock, and the interrupt subroutine requires the same operation. If the host wants to send multiple bytes, it can continue to send. The figure above only shows the case where the host sends a data.

Finally, the host sends a stop signal IIC_STOP after sending all the data, indicating the end of the communication, releasing the IIC bus, and the bus enters the idle state.

IIC host read timing diagram



IIC host does not pull low clock line diagram

As shown in the above figure, the schematic diagram of the clock line is not pulled when the host reads.

First the host sends a start signal IIC_START, marking the beginning of communication. As shown by the dotted line a. The internal circuit detects the IIC_START signal timing and sets the status flag IIC_START.

Then the host sends the address bytes and write flag bit, IIC_RW = 1, indicates that the host reads the slave. The slave automatically compares with its own address after receiving the address byte.Status bit IIC_RW set. As shown by the dotted line b. Set IIC_RW after the falling edge of the ninth clock if the address matches.

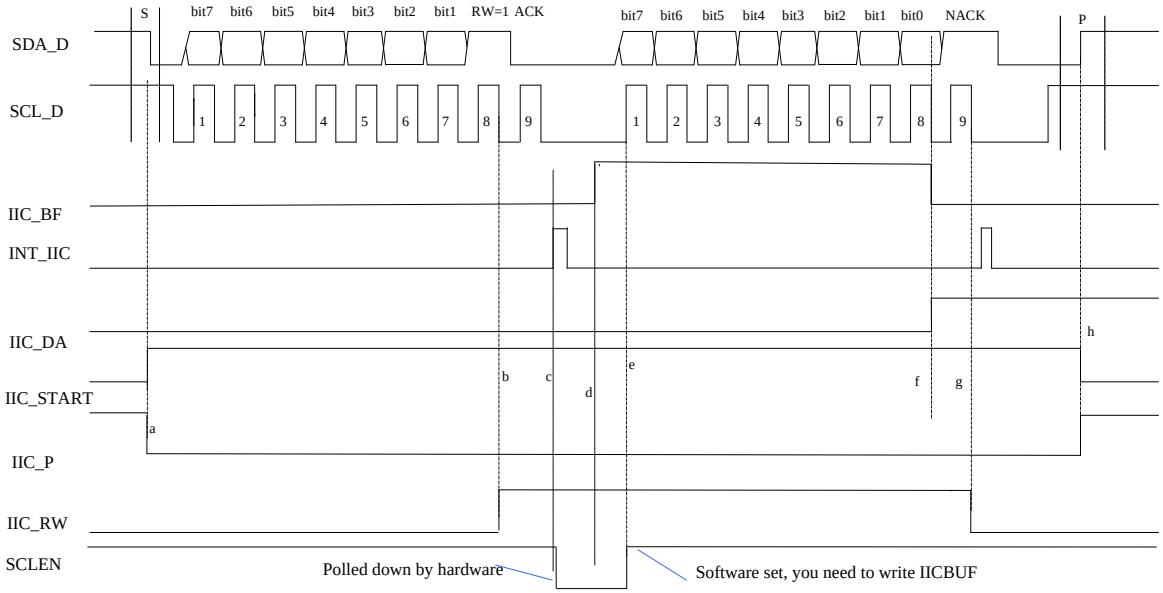
An interrupt signal INT_IIC is generated after the falling edge of the ninth clock. As shown by the dotted line c. Ballast the data in IICBUFFER to IICBUF, IIC is set to clear, as shown by the dotted line d, and the highest bit is sent to the bus. After the eighth clock, one byte of data is sent, IIC_BF is set to clear; At the same time, the address data flag will also be set, indicating the currently transmitted byte data.

As shown by the dotted line e. An interrupt signal INT_IIC is generated after the falling edge of the ninth clock.If the host needs to read the slave, the host replies with a valid acknowledge bit ACK and continues to communicate. If the data require by the host has been read, the host replies with an invalid response NACK, and then sends a stop signal IIC_STOP to stop the communication. This should be noted in the application. When the NACK is detected, the read/write flag IIC_RW is

cleared by hardware. As shown by the dotted line f. If the host sends a NACK, the slave SCLEN will not be automatically pulled low.

Finally, the host sends a stop signal IIC_STOP after reading all the data, indicating the end of the communication. When the IIC_STOP signal is detected the status bit IIC_STOP is set and IIC_START is cleared. Release IIC bus. As shown by the dotted line g. The bus enters the idle state.

IIC host read pull low timing diagram



IIC host read pull low clock line diagram

As shown in the above figure, the schematic diagram of the clock line is not pulled when the host reads.

First the host sends a start signal IIC_START, marking the beginning of communication. As shown by the dotted line a. The internal circuit detects the IIC_START signal timing and sets the status flag IIC_START.

Then the host sends the address byte after the IIC_START signal. IIC_RW = 1, indicates that the host reads the slave. Status bit IIC_RW set. As shown by the dotted line b. Will not be set if the addresses do not match.

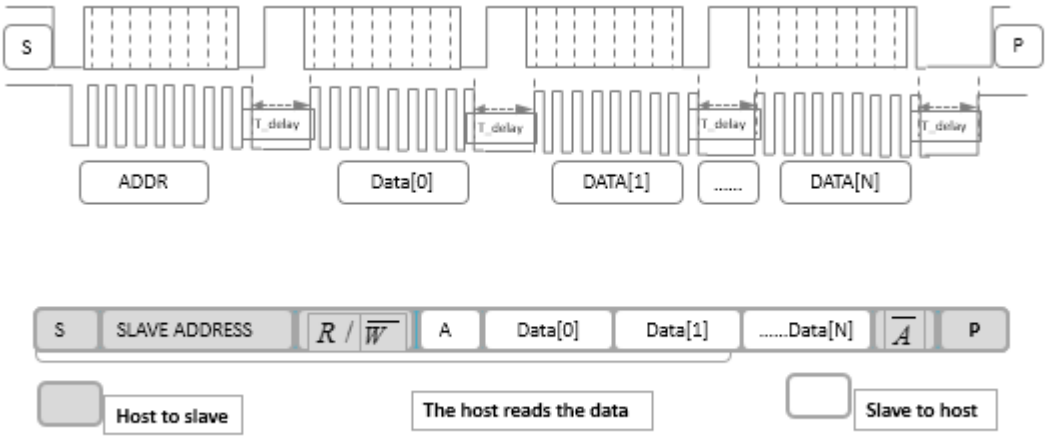
An interrupt signal INT_IIC is generated after the falling edge of the ninth clock. As shown by the dotted line c. SCLEN will also be automatically pulled low by the hardware after the falling edge of the ninth clock. This period is used to process or prepare data from the slave, then write the prepared data to IICBUF, set SCLEN in software, and release the clock line. As shown by the dotted line d. In writing the data to the IIC, the IIC will be set, indicating that the IIC is full at this time. As shown by the dotted line e.

After the master detects that the slave releases the SCL, it continues to send the synchronous clock and read the slave data. After the falling edge of the 8th clock, one byte of data has been sent and IIC_BF cleared; At the same time, the address data flag will also be set, indicating the currently transmitted byte data. As shown by the dotted line f.

An interrupt signal INT_IIC is generated after the falling edge of the ninth clock.If the host needs to continue to read the slave, the host replies with a valid acknowledge bit ACK and continues to communicate; If the data require by the host has been read, the host replies with an invalid response NACK, and then sends a stop signal IIC_STOP to stop the communication. When the NACK is detected, the read/write flag IIC_RW is cleared by hardware. As shown by the dotted line g.

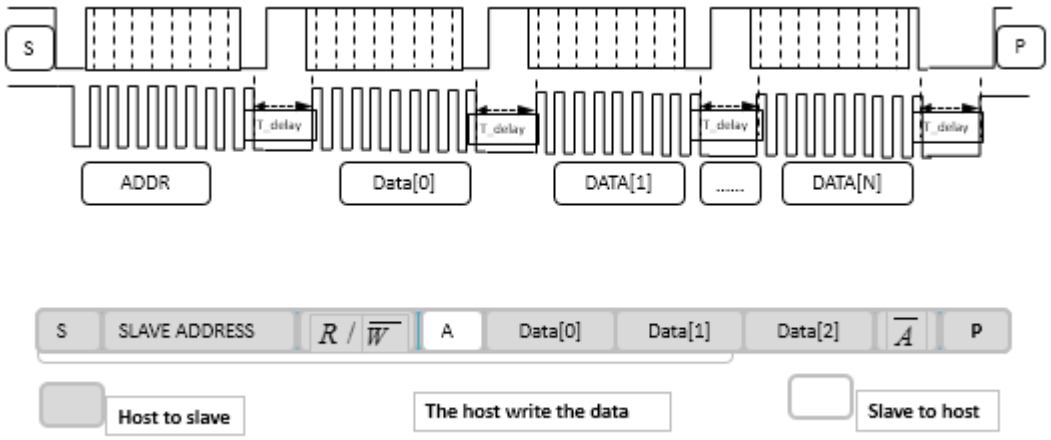
Finally, the host sends a stop signal IIC_STOP after reading all the data, indicating the end of the communication. When the IIC_STOP signal is detected the status bit IIC_STOP is set and IIC_START is cleared. Release IIC bus. As shown by the dotted line h. The bus enters the idle state.

IIC host read data diagram



PS: T_delay: Reserve slave interrupt time, generally 60us~300us, if the slave IIC interrupts the service processing time at100us, suggest T_delay>200us.

IIC host write data diagram



PS: T_delay: Reserve slave interrupt time, generally 60us~300us, if the slave IIC interrupts the service processing time at100us, suggest T_delay>200us .

At the eighth clock slave send ack, IIC interrupt occurs at the ninth clock fulling edge.It is recommended that the host delay 60us~300us when the ninth clock fulling edge is sent. Reserve the

slave IIC interrupt service data preparation time, and then send the clock signal.

Note: When IIC communication>=100K, it is recommended that the system clock is 6MHz.

9.2. IIC Related Register

SFR register				
Address	**Name**	**RW**	**Reset value**	**Description function**
0xE3	IICADD	RW	0000_000xb	IIC address register
0xE4	IICBUF	RW	0000_0000b	IIC transmit receive data register
0xE5	IICCON	RW	xx01_0000b	IIC configuration register
0xE6	IEN1	RW	0000_00xxb	Interrupt enable register 1
0xE8	IICSTAT	R/RW	0100_0100b	IIC status register
0xE9	IICBUFFER	RW	0000_0000b	IIC transmit and receive data buffer register
0xF1	IRCON1	RW	0000_00xxb	Interrupt flag register 1
0xF2	PERIPH_IO_SEL	RW	x100_0000b	IIC /INT function control register
0xF6	IPL1	RW	0000_00xxb	Interrupt priority register 1

IIC registers list

9.3. IIC Registers Detailed Description

9.3.1. IIC Register Detailed Description

IICADD (E3H) IIC address register

Bit number	7	6	5	4	3	2	1	0
Symbol	IICADD[7:1]							-
R/W	R/W							-
Reset value	0							-

Bit number	Bit symbol	Description
7~1	IICADD[7:1]	IIC address register

IICBUF (E4H) IIC transmit and receive data register

Bit number	7	6	5	4	3	2	1	0
Symbol	IICBUF							
R/W	R/W							
Reset value	0							

Bit number	Bit symbol	Description
7~0	IICBUF	IIC transmit receive data buffer

IICCON (E5H) IIC configuration register

Bit number	7	6	5	4
Symbol	–	–	IIC_RST	RD_SCL_EN
R/W	–	–	R/W	R/W
Reset value	–	–	0	1
Bit number	3	2	1	0
Symbol	WR_SCL_EN	SCLEN	SR	IIC_EN
R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0

Bit number	Bit symbol	Description
7~6	--	Reserved
5	IIC_RST	IIC module reset signal 1: IIC module reset operation 0: IIC module works properly
4	RD_SCL_EN	Host read pull low clock line control bit. 1: enable the host to read and pull the low clock line function; 0: disable the host to read and pull the low clock line function.
3	WR_SCL_EN	Host write pull low clock line control bit. 1: enable the host to write and pull the low clock line function; 0: disable the host to write and pull the low clock line function.
2	SCLEN	IIC clock enable bit 1: clock work properly 0: pull down the clock line.
1	SR	IIC conversion rate control bit 1: Conversion rate control is turned off to adapt to the standard speed mode (100K); 0: Conversion rate control is enabled to adapt to fast speed mode (400K)
0	IIC_EN	IIC work enable bit 1: IIC normal work; 0: IIC not work

IEN1 (E6H) Interrupt enable register 1

Bit number	7	6	5	4	3	2	1	0
Symbol	EX7	EX6	EX5	EX4	EX3	EX2	-	-
R/W	R/W	R/W	R/W	R/W	R/W	R/W	-	-
Reset value	0	0	0	0	0	0	-	-

Bit number	Bit symbol	Description
3	EX3	IIC interrupt enable

		1: interrupt enable; 0: interrupt disable

IICSTAT (E8H) IIC status register

Bit number	7	6	5	4
Symbol	IIC_START	IIC_STOP	IIC_RW	IIC_AD
R/W	R	R	R	R
Reset value	0	1	0	0
Bit number	3	2	1	0
Symbol	IIC_BF	IIC_ACK	IIC_WCOL	IIC_RECOV
R/W	R	R	R/W	R/W
Reset value	0	1	0	0

Bit number	Bit symbol	Description
7	IIC_START	Start signal flag 1: start bit detected; 0: no start bit detected
6	IIC_STOP	Stop signal flag 1: stop status detected; 0: no stop status detected
5	IIC_RW	Read and write flag. Record the read/write information obtained from the address byte after the last address match. 1: read; 0: write.
4	IIC_AD	Address data flag 1: The most recently received or sent byte is data; 0: The most recently received or sent byte is address
3	IIC_BF	IICBUF full flag. Received in IIC bus mode: 1: received successfully, buffer is full; 0: received successfully, buffer is empty. Send in IIC bus mode 1: data transmission is in progress (does not include the acknowledge bit and the stop bit), buffer is full; 0: data transmission has been completed (does not include the acknowledge bit and the stop bit), buffer is empty.
2	IIC_ACK	Answer flag 1: invalid response signal; 0: effective response signal.
1	IIC_WCOL	Write conflict flag. 1: when the IIC is transmitting the current data, the new data is attempted to be written to the transmit buffer; new data

		cannot be written to the buffer. 0: no write conflict
0	IIC_RECOV	Receive overflow flag bit 1: When the previous data received by the IIC has not been taken, new data is received, the new data cannot be received by the buffer. 0: no receive overflow.

IICBUFFER (E9H) IIC transmit and receive data buffer register

Bit number	7	6	5	4	3	2	1	0
Symbol	IICBUFFER							
R/W	R/W							
Reset value	0							

Bit number	Bit symbol	Description
7~0	IICBUFFER	IIC transmit receive data buffer register. RD_SCL_EN=0, when the host reads the data, the data in the IICBUFFER is send to the slave transmit buffer after 2 clocks after the interrupt is generated, the data sent as a salve. Therefore, the previously prepared IICBUFFER interrupt data is generated before the interruption.

IRCON1 (F1H) Interrupt flag register 1

Bit number	7	6	5	4	3	2	1	0
Symbol	IE7	IE6	IE5	IE4	IE3	IE2	-	-
R/W	R/W	R/W	R/W	R/W	R/W	R/W	-	-
Reset value	0	0	0	0	0	0	-	-

Bit number	Bit symbol	Description
3	IE3	IIC interrupt flag 1: There is a IIC interrupt flag; 0: No IIC interrupt flag

PERIPH_IO_SEL (F2H) IIC /INT function control register

Bit number	7	6	5	4	3
Symbol	-	IIC_AFIL_SEL	IIC_DFIL_SEL	IIC_IO_SEL	
R/W	-	R/W	R/W	R/W	R/W
Reset value	-	1	0	0	0
Bit number	2	1	0	/	
Symbol	INT2_IO_SEL	INT1_IO_SEL	INT0_IO_SEL	/	
R/W	R/W	R/W	R/W		
Reset value	0	0	0		

Bit number	Bit symbol	Description
6	IIC_AFIL_SEL	IIC port analog filter selection enable 1: select analog filter function; 0: do not select analog filter function.
5	IIC_DFIL_SEL	IIC port digital filter selection enable. 1: select digital filter function; 0: do not select digital filter function.
4~3	IIC_IO_SEL	IIC select enable 0: PA0/PA1 select IIC function; 1: PB5/PC0 select IIC function; 2: PA1/PD6 select IIC function (When PB5/PC0 is used as IIC port, there is no SR control function, automatic logic control becomes open-drain output, when PB5/PC0 is used as GPIO, there is no open-drain output function)

IPL1 (F6H) Interrupt priority register 1

Bit number	7	6	5	4	3	2	1	0
Symbol	IPL1.7	IPL1.6	IPL1.5	IPL1.4	IPL1.3	IPL1.2	-	-
R/W	R/W	R/W	R/W	R/W	R/W	R/W	-	-
Reset value	0	0	0	0	0	0	-	-

Bit number	Bit symbol	Description
3	IPL1.3	IIC interrupt priority. 0: low priority; 1: high priority

9.3.2. IICSTAT Register

The IIC status register is used to reflect the status in the communication process and can be inquired by the user. Bit0 and Bit1 are readable and writable, and the other bits are read-only.

IICSTAT (E8H) IIC status register

Bit number	7	6	5	4
Symbol	IIC_START	IIC_STOP	IIC_RW	IIC_AD
R/W	R	R	R	R
Reset value	0	1	0	0
Bit number	3	2	1	0
Symbol	IIC_BF	IIC_ACK	IIC_WCOL	IIC_RECOV
R/W	R	R	R/W	R/W
Reset value	0	1	0	0

Bit number	Bit symbol	Description
7	IIC_START	Start signal flag 1: start bit detected; 0: no start bit detected
6	IIC_STOP	Stop signal flag 1: stop status detected; 0: no stop status detected
5	IIC_RW	Read and write flag. Record the read/write information obtained from the address byte after the last address match. 1: read; 0: write.
4	IIC_AD	Address data flag 1: The most recently received or sent byte is data; 0: The most recently received or sent byte is address
3	IIC_BF	IICBUF full flag. Received in IIC bus mode: 1: received successfully, buffer is full; 0: received successfully, buffer is empty. Send in IIC bus mode 1: data transmission is in progress (does not include the acknowledge bit and the stop bit), buffer is full; 0: data transmission has been completed (does not include the acknowledge bit and the stop bit), buffer is empty.
2	IIC_ACK	Answer flag 1: invalid response signal; 0: effective response signal.

1	IIC_WCOL	Write conflict flag. 1: when the IIC is transmitting the current data, the new data is attempted to be written to the transmit buffer; new data cannot be written to the buffer. 0: no write conflict
0	IIC_RECOV	Receive overflow flag bit 1: When the previous data received by the IIC has not been taken, new data is received, the new data cannot be received by the buffer. 0: no receive overflow.

IIC_START: Start signal status bit, IIC_START is set when the start signal is detected, Indicating that the bus is busy.

IIC_STOP: Stop signal status bit, IIC_START is set when the start signal is detected, indicating that the bus is idle. When the start signal is detected, the hardware is cleared, indicating that communication begins.

IIC_AD: Address data flag. It indicates whether the byte currently received or sent is an address or data. IIC_AD =0, flag is currently received or sent byte is the address; IIC_AD = 1 flag is currently received or sent byte is the data; Start signal, stop signal, non-response signal have no effect on this status bit. This status bit change occurs on the falling edge of the eighth clock.

IIC_RW: Read and write flag. The flag bit is recorded the read and write information bits obtained from the address is matched. IIC_RW = 1 means the host reads the slave. RW = 0 means the host writes the slave. Start signal, stop signal, non-answer signal (NACK) is cleared IIC_RW. This status bit change occurs on the falling edge of the ninth clock.

IIC_BF: BUFFER full flag. It indicates that the transceiver buffer is currently full or empty. IIC_BF=0 indicates that the buffer does not receive data and the buffer is empty; IIC_BF=1 indicates that the buffer receive data and the buffer is full. This status bit can only be set and cleared indirectly, not directly.

Address matching and IIC_RW = 0, IIC_BF will be set after the falling edge of the eighth clock, indicating that the IICBUF has received the data. The IICBUF should be read during the execution of the interrupt routine, and the read IICBUF will indirectly clear the BF flag. If the host does not read IICBUF and the host continues to send data, a receive overflow will occur. Although the slave still receives the host to send data and is ballasted to the IICBUF.

IIC_RW=1 indicates the operation of the master to read the slave, the slave operation needs to write data to the IICBUF, and the slave writes IICBUF operation to set the IICBUF. The software then sets SCLEN to release the clock line. The host The host sends the synchronous clock. After the 8th clock is passed, the IICBUF is cleared by hardware after the data in the IICBUF is sent out.

IIC_ACK: Answer flag. Regardless of whether the host is a read or write operation, the slave samples the data line from the rising edge of the ninth clock and records the response information. The acknowledge bits are divided into a valid acknowledgment ACK and a non-valid acknowledgement bit NACK. That is to say, the rising edge of the ninth clock samples the data to 0,

indicating that the ACK is valid, and the IIC_ACK is cleared. If data 1 is sampled, NACK is set, indicating non-response. After the non-acknowledgment signal, the host will send a stop signal to announce the end of the communication. The start signal will clear this status bit.

IIC_WCOL: Write conflict flag. IICBUF only when IIC_RW=1, RD_SCL_EN=1 and SCLEN = 0 can be written by the CPU. Any other attempt to write to IICBUF is forbidden. If the above conditions are not met, the write IICBUF operation occurs. Then the data will not be written to IICBUF, and the conflict flag IIC_WCOL will be set. This flag needs to be cleared by software.

IIC_RECOV: Receive overflow flag.In the case of IICBUF full, that is, in the case of data in the IICBUF. If IIC received new data, it will receive overflow and IIC RECOV will set.At the same time, the data in the IICBUF will not be updated, and the newly received data will be lost. This status bit also requires software to clear, otherwise it will affect the subsequent communication. This kind of situation will only appear in IICRW=0. BF=1, and the CPU will appear when it does not read IICBUF.

9.3.3. CON Register

The IICCON register is used to control the communication operation.

IICCON (E5H) IIC configuration register

Bit number	7	6	5	4
Symbol	–	–	IIC_RST	RD_SCL_EN
R/W	–	–	R/W	R/W
Reset value	–	–	0	1
Bit number	3	2	1	0
Symbol	WR_SCL_EN	SCLEN	SR	IIC_EN
R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0

Bit number	Bit symbol	Description
7~6	--	Reserved
5	IIC_RST	IIC module reset signal 1: IIC module reset operation 0: IIC module works properly
4	RD_SCL_EN	Host read pull low clock line control bit. 1: enable the host to read and pull the low clock line function; 0: disable the host to read and pull the low clock line function.
3	WR_SCL_EN	Host write pull low clock line control bit. 1: enable the host to write and pull the low clock line function; 0: disable the host to write and pull the low clock line function.
2	SCLEN	IIC clock enable bit 1: clock work properly

		0: pull down the clock line.
1	SR	IIC conversion rate control bit 1: Conversion rate control is turned off to adapt to the standard speed mode (100K); 0: Conversion rate control is enabled to adapt to fast speed mode (400K)
0	IIC_EN	IIC work enable bit 1: IIC normal work; 0: IIC not work

The role is describle in detail below:

IICEN is module enable signal, when IICEN=1, the circuit works.

SR is the conversion rate control bit, SR=1 conversion ratecontrol off, port adapted to 100Kbps communication.

SCLEN is clock enable control bit, although the slave cannot generate the communication clock, the slave can extend the low time of the clock according to the protocol. SCLEN=0, clock line is locked at low level; SCLEN=1, release clock line. The premise of extending the low level of the clock is IICEN=1, otherwise the internal circuit will not have any effect on the IIC bus. SCLEN is often used to extend low time and make the host enter the wait state, so that the slave has enough time to process the data.

WR_SCL_EN is write low line control bit. When it is 1 to enable the interrupt to pull down the clock line, when it is 0, it does not enable the interrupt to pull down the clock line.

IIC_RW=0, according to the communication rate of the host and the time of processing the interrupt, it is determinded whether to lower the clock line, that is, configure the WR_SCL_EN bit.

When the CPU can process the interrupt and exit the interrupt within 8 IIC clocks. WR_SCL_EN=0 disable pull down the clock clock line function. At this time, the hardware will not automatically pull down the clock line when the interrupt arrives. When the CPU cannot process the interrupt and exit in the 8 IIC clocks, WR_SCL_EN=1 enables the clock line to be pulled down. At this point, the hardware automatically pulls down the clock line when the interrupt arrives, forcing the host to enter the wait state. When the data written to the IIC is read by the CPU, the software sets SCLEN.

RD_SCL_EN is read low line control bit. When it is 1 to enable the interrupt to pull down the clock line, when it is 0, it does not enable the interrupt to pull down the clock line.

RD_SCL_EN=1, when the slave receives the address byte or sends one byte and the host sends, SCLEN wll be automatically pulled low by hardware, forcing the host to the enter the wait state. The release the IIC clock from the slave, the following two operations arerequired: first write the data to be sent to the IIC, set the software in IICBUF in SCLEN. The purpose of this design is to ensure that the data to be sent has been written in the IICBUF before the SCL is pulled high.

RD_SCL_EN=0, when the slave receives the address byte or sends one byte and the host sends an ACK, the slave immediately polls the data prepared in the IICBUFFER register to the transmit buffer register and then to the data line. Therefore, in order to ensure that data transmitted each time

is correct, IICBUFFER prepares the next data to be sent in the interrupt service routine. The data received by the host is the last interrupted data, and the first time the data is received is ready for initialization.

Note: When you need to pull down the clock line, that is, WR_SCL_EN/RD_SCL_EN=1. Software should turn off the clock line until the last Byte data is sent and received. That is, WR_SCL_EN/RD_SCL_EN=0, the software should turn on the write low pull clock line before sending and receiving the last Byte data. This kind of operation can be self-regulated according to whether the host is software or hardware.

IIC_RST is IIC module control enable bit, enable the IIC module reset function for 1 and disable the IIC module reset function when 0. Pay attention to configuration 1 reset IIC module all DFF triggers. The reset terminal of IIC_RST is global reset, and the other reset terminal are iic_rst_n. All iic_rst writes 0 first, then operate other register configurations.

9.3.4. IICBUF Register

The IICBUF register is used to control the communication operation.
IICBUF (E4H) IIC transmit and receive data register

Bit number	7	6	5	4	3	2	1	0
Symbol	IICBUF							
R/W	R/W							
Reset value	0							

Bit number	Bit symbol	Description
7~0	IICBUF	IIC transmit and receive data buffer

The specific application process is as follows:

In the send state, after the data is ballasted into the IICBUF, under the synchronous clock of the host. The data is sequentially shifted and sent out, the high position is in front. After 8 clocks, one byte is sent.

In the receive state, after the host's 8 clocks have passed, the data is written to the BUF. After the 9th clock, an interrupt is generated, telling the CPU to read the data in the IICBUF.

Writing data to IICBUF is conditional, when RD_SCL_EN=1, only IIC_RW=1, and SCLEN=0 can write data into IICBUF; Otherwise, the operation of writing IICBUF is prohibited. That is to say, if the condition is not satisfied, the operation of writing IICBUF cannot be successful, and the data cannot be written. IICBUF data will not change, but will also cause write confilicts.

For example: IICBUF already has been 55h. In case the condition of writing IICBUF is not satisfied, we want to write data 00h into IICBUF. The result is that the data in IICBUF is still 55h, and the write conflict flag IIC_WCOL is set to tell the user that the operation is abnormal.

When RD_SCL_EN=0, the data to be the slave is the value of the ballast IICBUFFER register when the interrupt signal is generated.

9.3.5. IICBUFFER Register

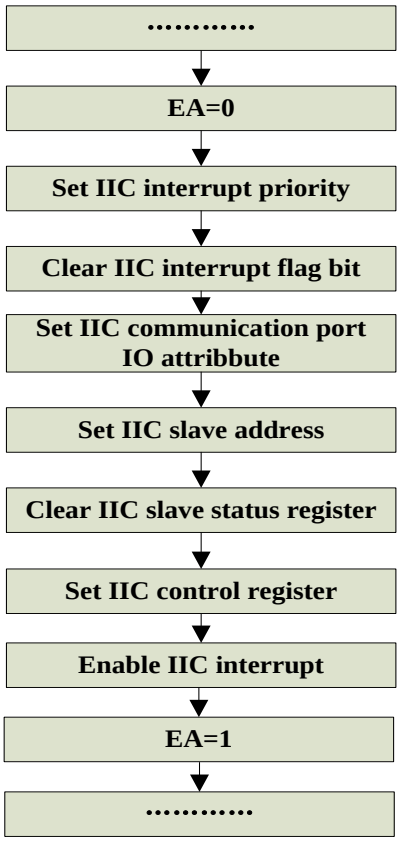
IICBUFFER (E9H) IIC transmit and receive data buffer register

Bit number	7	6	5	4	3	2	1	0
Symbol	IICBUFFER							
R/W	R/W							
Reset value	0							

The specific application process is as follows:

When RD_SCL_EN=0, and the host reads the data, the data in the IICBUFFER is sent to the slave transmit buffer register after the two clks after the interrupt is generated, and the data is sent as slave. Therefore, the data in the IICBUFFER should be prepared before the interrupt is generated. Generally, it is ready in the service routine. Device address generation interrupts send data to prepare for initialization.

9.4. IIC Configure Process



IIC configure process

Notes: IIC bus pull-up resistor 4.7k~10k, ground filter capacitor 10pF~ 100pF close to the lead chip.

10. UART

There are 2 UART modules in the BF7812AMXX-XJLX series. UART0 supports 5 IO port mapping, and UART1 supports 3 channels. Only one set of mapping can be mapped at the same time. UART module interface characteristics:

- Support full-duplex, half-duplex serial
- Independent dual buffer receiver and single buffer transmitter
- Programmed baud rate (10bit analog-to digital divider)
- Interrupt-driven or polling operation:
  - send completed
  - receiving full
  - receive overflow, parity error, frame error
- Supports hardware parity production and check
- Programmable 8bit or 9bit character length
- STOP bit 1 or 2 can be selected
- Supports multiprocessor mode
- Support TXD/RXD pin position swap
- Support TXD/RXD independent enable

10.1. UART Function Description

10.1.1. Baud Rate Generation

Baud rate generation modules: Baud_Mod= {UART0/1_BDH[1:0], UART0/1_BDL}.

Baud rate calculation formula: Baud_Mod=0, does not generate baud rate clock. When Baud_Mod=1~1023, UART0 baud rate = BUSCLK/(16x Baud_Mod).

The BUSCLK uses the divided clock of the system clock source, fixed to 24M. Each time the baud rate register is configured, the internal counter is cleared and the baud rate signal is regenerated. Communication requires the transmitter and receiver to use the same baud rate. Baud rate deviation range allowed by communication: 8/(11*16)=4.5%.

10.1.2. Transmitter Function

Send data flow: Trammitted by writing UART0/1_BUF data, sending stop bit after sending stop bit. Software clear interrupt flag and waits for the next write. The transmitter output pin (TXD) idle state defaults to a logic high state. The entire transmission process must be performed when the module is enabled.

By writing data to the data register (UART0/1_BUF), save the data directly to the send data buffer and start the send process. The data buffer is locked during the subsequent complete transmission.The configuration write data register UART0/1_BUF and T8 is invalid. After the stop bit is sent, writing to UART0/1_BUF again will restart the new transmission.

The serial component of the serial transmitter has a length of 10/11/12 (depending on the setting in the data_mode control bit) transmit shift register. If data_mode=0, select normal 8bit data mode. In the 8bit data mode, there is 1 start bit in the shift register, 8 data bits and 1/2 stop bits. Send and receive are small endian mode (LSB first).

10.1.3. Receiver Function

The receiver is enabled by setting the receive enable bit in UART0/1_CON1. The entire receiving process must be performed when the module is enabled.

Receiving data flow: receive data at any time with the reception enable enabled. After receiving the stop bit, set the middle segment and the software clears the interrupt flag.

Currently acceptly data will detect wit, detect receive overflow, frame error, parity error three errors. Software clearance mark required. It is recommended to read the status flag and read the data buf after receiving the receive interrupt. Finally, the received data status flags are cleared.

Data character is started by logic 0, 8 or 9 data bit (LSB send first) and stop bits (1bit) of logic 1. After receiving the stop bit to the shifter, if the receive data shift register is not full (RI0/1=0), data characters are transferred to the receive data register, setting the receive data register full (RI0/1=1) status flag. If the rx_full_if of the receive data register is already set at this time, set the overflow (UART0/1_RO) status flag, the new data will be lost. Because the receiver is double

buffered, after setting rx_full_if, program has a full character time for reading before reading the data of the receive data buffer to avoid receiver overflow.

When the program detects that the receive data register is full (RI0/1=1), it acquires data from the receive data register by reading UART0/1_BUF.

10.1.4. Receiver Sampling Method

The receiver uses with a 16x baud rate clock for sampling. The receiver searches for falling edge on the RXD serial data input pin by extracting the logic level samples at 16x baud rate.The falling edge is defined as the logic 0 level after 3 consecutive logic 1 samples. The 16x baud rate clock is used to divide the bit time into 16 segements, labeled RT1 and RT16 respectively.

The receiver then samples at each bit time of RT8, RT9 and RT10, including the start and stop bits to determine the logic level of the bit. The logic level is the logic level of most samples advanced during the bit time period. When the falling edge is located, the logic level is 0 to ensure that this is the true starting bit, not the noise. If at least two of the three samples are 0, the receiver assumes that it is synchronized with the receiver character. Start shifting to receive the following data, if the above conditions are not met, exit the state machine and return to the waiting for falling edge state.

The falling edge detection logic constantly looks for the falling edge. If an edge is detected, the sample clock resynchronizes the bit time. This improves the reliability of the receiver when noise or mismatch in baud rate occurs.

10.1.5. Multiprocessor Mode

Multiprocessor mode, only works in 9-bit mode, when the received UART0/1_R8 bit=1, the receive interrupt is set, otherwise it is not set. The role of this mechanism is to eliminate the software overhead of handing unimportant information for diffrernt receivers.

In this application system, all receivers estimate the address character (ninth bit=1) of each message. Once it is determined that the information is intended for different receivers, subsequent data characters (ninth bit=0) are not received.

Configuration process: configuring receive enable, configuring multiprocessor mode, received address data (ninth bit=1), receive and generate an interrupt. The application confirms that the addresses match, and the match configures to turn off the multiprocessor mode. All subsequent data (ninth bit=0) can be received and interrupted until the next time the address data is received, the address does not match, then the multiprocessor mode is turned on. Then all subsequent data is not received until the next address data, and then cyclically applied.

10.2. UART Related Register

SFR register				
Address	**Name**	**RW**	**Reset value**	**Function description**
0xBD	UART0_BDL	RW	0000_0000b	UART0 Baudrate control register
0xBE	UART0_CON1	RW	0000_0000b	UART0 control register 1
0xBF	UART0_CON2	RW	xxx0_1100b	UART0 control register 2
0xC0	UART0_STATE	R/RW	x000_0000b	UART0 status flag register
0xC1	UART0_BUF	RW	1111_1111b	UART0 data register
0xC5	UART1_BDL	RW	0000_0000b	UART1 baud rate control register
0xC6	UART1_CON1	RW	0000_0000b	UART1 control register 1
0xC7	UART1_CON2	RW	xxx0_1100b	UART1 control register 2
0xC8	UART1_STATE	R/RW	x000_0000b	UART1 status flag register
0xC9	UART1_BUF	RW	1111_1111b	UART1 data register
0xE1	IRCON2	RW	xxxx_0000b	Interrupt flag register 2
0xE7	IEN2	RW	xxxx_0000b	Interrupt enable register 2
0xEE	UART_IO_SEL	RW	xxx0_0000b	UART select enable register
0xF4	IPL2	RW	xxxx_0000b	Interrupt priority register 2

UART registers list

10.3. UART Register Detailed Description

UART0_BDL (BDH) UART0 Baudrate control register

Bit number	7	6	5	4	3	2	1	0
Symbol	-							
R/W	R/W							
Reset value	0							

Bit number	Bit symbol	Description
7~0	--	Baud rate control register. Baud rate modules divisor register lower 8 bits, bandrate={UART0_BDH[1:0], UART0_BDL}, bandrate=0, does not generate baud rate clock. bandrate=1~1023, bandrate = BUSCLK/(16xBaud_Mod)

UART0_CON1 (BEH) UART0 control register 1

Bit number	7	6	5	4
Symbol	UART0_ ENABLE	TRANS_ ENABLE	RECEIVE_ ENABLE	MULTI_ MODE
R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0
Bit number	3	2	1	0
Symbol	STOP_MODE	DATA_MODE	PARITY_EN	PARITY_SEL
R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0

Bit number	Bit symbol	Description
7	UART0_ENABLE	Module enable. 1: module enable; 0: module off.
6	TRANS_ENABLE	Transmitter enable 1: transmitter is on; 0: transmitter is off
5	RECEIVE_ENABLE	Receiver enable. 1: receiver open; 0: receiver off.
4	MULTI_MODE	Multiprocessor communication mode. 1: mode enable; 0: mode disable.
3	STOP_MODE	Stop bit width selection. 1: 2 bit; 0: 1 bit.
2	DATA_MODE	Data mode select. 1: 9bit mode; 0: 8bit mode.
1	PARITY_EN	Parity enable. 1: parity enable; 0: parity disable.
0	PARITY_SEL	Parity select. 1: odd parity; 0: even parity.

UART0_CON2 (BFH) UART0 control register 2

Bit number	7~5	4	3	2	1	0
Symbol	-	PAD_CHANGE	TX_EMPTY_IE	RX_FULL_IE	UART0_BDH	
R/W	-	R/W	R/W	R/W	R/W	
Reset value	-	0	1	1	0	0

Bit number	Bit symbol	Description
4	PAD_CHANGE	Txd/rxd pin interchange 1: pin interchange; 0: the pins are not interchangeable
3	TX_EMPTY_IE	Send interrupt enable. 1: interrupt enable; 0: interrupt disable (used in polling mode)
2	RX_FULL_IE	Received interrupt enable 1: interrupt enable; 0: interrupt disable (used in polling mode)
1~0	UART0_BDH	Baud rate modulus divisor register high 2bit.

UART0_STATE (C0H) UART0 status flag register

Bit number	7	6	5	4
Symbol	-	UART0_R8	UART0_T8	TI0
R/W	-	R	R/W	R/W
Reset value	-	0	0	0
Bit number	3	2	1	0
Symbol	RI0	UART0_RO	UART0_F	UART0_P
R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0

Bit number	Bit symbol	Description
6	UART0_R8	Receiver’s ninth data, read only.
5	UART0_T8	Transmitter’s ninth data, read only when parity is enabled.
4	TI0	Send interrupt flag. 1: send buffer is empty; 0: send buffer is full, software write 0 clear 0, write 1 invalid.
3	RI0	Receive interrupt flag. 1: receive buffer is full; 0: receive buffer is empty, software write 0 clear 0, write 1 invalid.
2	UART0_RO	Receive overflow flag; 1: receive overflow (lost new data); 0: no overflow, software write 0 clear 0, write 1 invalid.
1	UART0_F	Framing error flag. 1: framing error flag; 0: no framing error flag, software write 0 clear 0, write 1 invalid.

0	UART0_P	Parity error flag. 1: receiver parity error; 0: parity is correct, software write 0 clear 0, write 1 invalid.

UART0_BUF (C1H) UART0 data register

Bit number	7	6	5	4	3	2	1	0
Symbol	-							
R/W	R/W							
Reset value	FF							

Bit number	Bit symbol	Description
7~0	--	Data register Read returns read-only receive data buffer contents, write into write-only send data buffer.

UART1_BDL(C5H) UART1 baud rate control register

Bit number	7	6	5	4	3	2	1	0
Symbol	-							
R/W	R/W							
Reset value	0							

Bit number	Bit symbol	Description
7~0	-	Baud rate control register The lower 8 bits of the baud rate modulus divisor register, Baud_Mod={UART1_BDH[1:0], UART1_BDL}, When Baud_Mod=0, the baud rate clock is not generated, when Baud_Mod=1~1023, the baud rate = BUSCLK/(16xBaud_Mod)

UART1_CON1 (C6H) UART1 control register 1

Bit number	7	6	5	4
Symbol	UART1_ ENABLE	TRANS_ ENABLE	RECEIVE_E NABLE	MULTI_ MODE
R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0
Bit number	3	2	1	0
Symbol	STOP_MODE	DATA_MODE	PARITY_EN	PARITY_SEL
R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0

Bit number	Bit symbol	Description
7	UART1_ENABLE	Module enable 1: module enable; 0: module close
6	TRANS_ENABLE	Transmitter enable 1: transmitter is on; 0: transmitter is off
5	RECEIVE_ENABLE	Receiver enable 1: receiver is on; 0: receiver is off
4	MULTI_MODE	Multiprocessor communication mode 1: mode enable; 0: mode disable
3	STOP_MODE	Stop bit width selection 1: 2 bits; 0: 1 bit
2	DATA_MODE	Data mode selection 1: 9-bit mode; 0: 8-bit mode
1	PARITY_EN	Parity check enable 1: parity check is enabled; 0: parity check is disabled
0	WAKE_SEL	Parity selection 1: odd parity; 0: even parity

UART1_CON2(C7H) UART1 control register 2

Bit number	7	6	5	4
Symbol	-	-	-	PAD_CHANGE
R/W	-	-	-	R/W
Reset value	-	-	-	0
Bit number	3	2	1	0
Symbol	TX_EMPTY_IE	RX_FULL_IE	UART1_BDH	
R/W	R/W	R/W	R/W	R/W
Reset value	1	1	0	0

Bit number	Bit symbol	Description
4	PAD_CHANGE	Txd/rxd pin interchange 1: pin interchange; 0: the pins are not interchangeable
3	TX_EMPTY_IE	Transmit interrupt enable 1: interrupt enable; 0: interrupt disabled (used in polling mode)
2	RX_FULL_IE	Receive interrupt enable 1: interrupt enable; 0: interrupt disabled (used in polling mode)
1~0	UART1_BDH	Baud rate modulus divisor register high 2 bits

UART1_STATE (C8H) UART1 status flag register

Bit number	7	6	5	4
Symbol	-	UART1_R8	UART1_T8	TI1
R/W	-	R	R/W	R/W
Reset value	-	0	0	0
Bit number	3	2	1	0
Symbol	RI1	UART1_RO	UART1_F	UART1_P
R/W	R/W	R/W	R/W	R/W

Bit number	Bit symbol	Description
6	UART1_R8	The 9th data of the receiver, read only
5	UART1_T8	The 9th data of the transmitter, read only during parity check
4	TI1	Send buffer empty interrupt flag 1: The sending buffer is empty; 0: Send buffer is full, software write 0 to clear
3	RI1	Receive interrupt flag 1: The receive buffer is full; 0: Receive buffer is empty, software write 0 to clear
2	UART1_RO	Receive overflow flag 1: Receive overflow (new data is lost); 0: No overflow, software writes 0 to clear
1	UART1_F	Frame error flag 1: A frame error is detected; 0: No frame error is detected, software writes 0 to clear
0	UART1_P	Parity error flag 1: Receiver parity error; 0: Parity check is correct, software writes 0 to clear

UART1_BUF (C9H) UART1 data register

Bit number	7	6	5	4	3	2	1	0
Symbol	-							
R/W	R/W							
Reset value	0							

Bit number	Bit symbol	Description
7~0	-	Read returns the contents of the read-only receive data buffer, writes to the write-only send data buffer.

IRCON2 (E1H) Interrupt flag register 2

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	IE11	IE10	IE9	IE8
R/W	-	-	-	-	R/W	R/W	R/W	R/W
Reset value	-	-	-	-	0	0	0	0

Bit number	Bit symbol	Description
2	IE10	UART1 interrupt flag 1: There is a UART1 interrupt flag; 0: No UART1 interrupt flag
1	IE9	UART0 interrupt flag 1: There is a UART0 interrupt flag; 0: No UART0 interrupt flag

IEN2(E7H) Interrupt enable register 2

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	EX11	EX10	EX9	EX8
R/W	-	-	-	-	R/W	R/W	R/W	R/W
Reset value	-	-	-	-	0	0	0	0

Bit number	Bit symbol	Description
2	EX10	UART1 interrupt enable 1: interrupt enable; 0: interrupt disable
1	EX9	UART0 interrupt enable 1: interrupt enable; 0: interrupt disable

UART_IO_SEL(EEH) UART select enable register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	UART1_IO_SEL		UART0_IO_SEL		
R/W	-	-	-	R/W	R/W	R/W	R/W	R/W
Reset value	-	-	-	0	0	0	0	0

Bit number	Bit symbol	Description
4~3	UART1_IO_SEL	UART1 port selection enable 00: PB1/2 (RXD1_A/TXD1_A) port select UART1 function 01: PB6/7 (RXD1_B/TXD1_B) port select UART1 function 1x: PD4/5 (RXD1_C/TXD1_C) port select UART1 function
2~0	UART0_IO_SEL	UART0 port selection enable 000: PA0/1 (RXD0_A/TXD0_A) port select UART0 function 001: PB3/4 (RXD0_B/TXD0_B) port select UART0 function

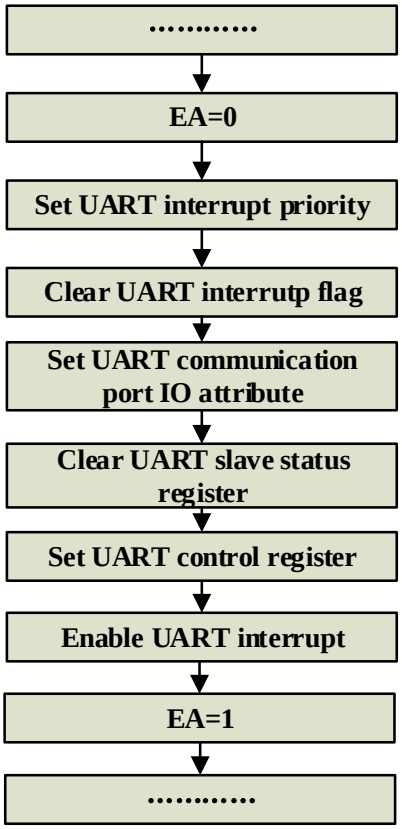
		010: reserved 011: PC0/1 (RXD0_D/TXD0_D) port select UART0 function 100: PD6/PA1 (RXD0_E/TXD0_E) port select UART0 function 101: PD7/PA0 (RXD0_F/TXD0_F) port select UART0 function

IPL2 (F4H) Interrupt priority register 2

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	IPL2.3	IPL2.2	IPL2.1	IPL2.0
R/W	-	-	-	-	R/W	R/W	R/W	R/W
Reset value	-	-	-	-	0	0	0	0

Bit number	Bit symbol	Description
7~4	--	Reserved
2	IPL2.2	UART1 interrupt priority. 0: low priority; 1: high priority
1	IPL2.1	UART0 interrupt priority. 0: low priority; 1: high priority

10.4. UART Configuration Process



UART initial configuration process

UART suggested application process:

1. Configuration module enable, receive enable, mode select: UART0/1_CON1;
2. Configure baudrate, open interrupt enable: UART0/1_BDL, UART0/1_CON2;
3. Write UART0_BF starts to send data, after detecting the transmission interrupt, clear the interrupt flag TI0;
4. Receive interrupt detected, first read status UART0/1_STATE. Then read R8 and UART0_BUF, finally clear the receive status flag (UART0_STAT[3:0] = 0). One receiving process is completed, waiting for the next receiving interrupt;
5. If the configuration interrupt is not enabled, the program executes the UART0/1function. Also read the status flag first, then read UART0/1_R8 and UART0_BUF, and finally clear the status flag.
6. Interrupt flag clear operation. In full-duplex operation, clear flag bit operation requires a vaild interrupt bit to be written 0, and other interrupt bits to be written as 1 (write 1 as invalid operation), otherwise it is easy to operate incorrectly. For example: when the send interrupt is vaild, you need tp write UART0_STATE = 0x0F; (configuration UART0/1_STATE[0:3] = 0x0F, UART0/1_R8 write is invalid, UART0/1_T8 needs to configure vaild transmit data when

it is in 9 bit mode and does not have parity).

7. 8 bit mode: Parity enable is valid.
   9 bit mode: When the parity bit is enabled, when the parity bit calculated by the ninth bit is not enable, the ninth bit is the UART0_T8 written in. Only send interrupts and receive interrupts.The error flag only marks the error detection of the current data, and only the corresponding bit writes 0 clear, do not jump out of error interrupt. The transmit interrupt is set after the stop bit is sent, and the software clears it. The receive interrupt is set after the stop bit is sent, and the software clears it.

   Multiprocessor mode: Only works in 9 bit mode, received UART0/1_R8= 1, receive interrupt is set, otherwise it is not set. When using multiprocessor mode, configuring receive enable and multiprocessor mode. Receive address data (the ninth bit=1) and generate an interrupt, confirm that the address matches. Matching configures the multiprocessor mode to be turned off, and all subsequent data (the ninth bit = 0) can be interrupted by the received interrupt, until the next time data is received. If the address do not match, the multiprocessor mode is turned on, and all subsequent data is not received until the next address data.

   Hardware response: Send data is opened by the value written to UART0/1_BUF. The interrupt flag is sent after the stop bit is sent. The software clears the interrupt flag and waits for the next write. The receive data receives data at any time when the receiving enable is effective. Set receive interrupt after receiving stop bit, software clear interrupt flag. The currently received data has a detection mechanism that can detect three errors of receive overflow, frame error, and parity error. Both require a software clear flag. It is recommended to read the status flag after the receive interrupt and clear the receive status flag UART0/1_STATE[0:3].
   Note: The mapping synchronization output function is not supported.

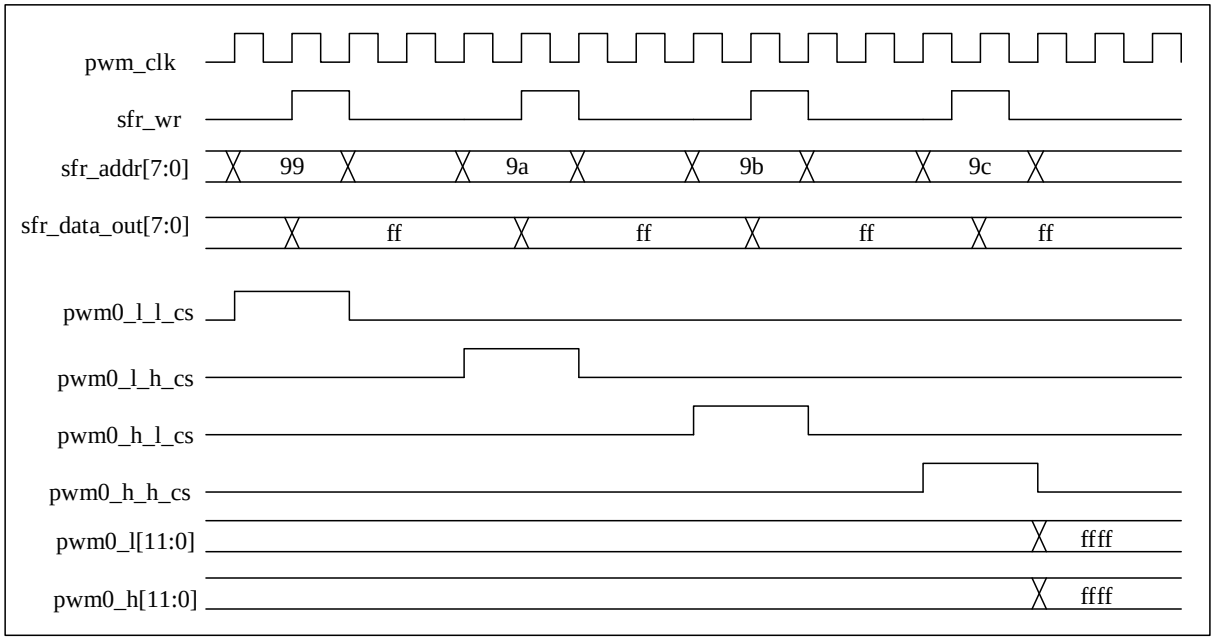
11. PWM

11.1. PWM Function Description

PWM0 Function Description:

- The clock source is PLL_24M;
- The high-level control register and the low-level control register are 12-bit registers;
- Output cycle: Tpwm_data = (PWM_H+PWM_L)*T prescaler time
- Output duty cycle: Dpwm_data = PWM_H / (PWM_H+PWM_L)
- PWM0 supports 1 channel output, PWM0_IO_SEL configuration mapping
- PWM1 supports 2-channel output with shared cycle, duty cycle and selectable polarity
- Support common frequency: 38kHz (infrared application, 1.7/2.3/3.0MHz (atomization frequency tracking application)

The cycle and pulse width of the PWM pulse width modulation module can be configured through registers, but the configuration of the registers must be in the case of PWM enable (active high), and the high-level control register and low-level control register must follow from The low-to-high sequence configuration is to ensure that the internal counter of the PWM module counts correctly and avoid generating wrong waveforms. These configuration values update the cycle and duty cycle after a complete period.



PWM register configuration timing diagram

11.2. PWM Related Registers

SFR register				
address	**name**	**R/W**	**Reset value**	**Description**
0x99	PWM0_L_L	RW	xxxx_0000b	PWM0 low level control register (low 4 bits)
0x9A	PWM0_L_H	RW	0000_0000b	PWM0 low level control register (high 8 bits)
0x9B	PWM0_H_L	RW	xxxx_0000b	PWM0 high level control register (low 4 bits)
0x9C	PWM0_H_H	RW	0000_0000b	PWM0 high level control register (high 8 bits)
0x9D	PWM1_L_L	RW	xxxx_0000b	PWM1 low level control register (low 4 bits)
0x9E	PWM1_L_H	RW	0000_0000b	PWM1 low level control register (high 8 bits)
0x9F	PWM1_H_L	RW	xxxx_0000b	PWM1 high level control register (low 4 bits)
0xA1	PWM1_H_H	RW	0000_0000b	PWM1 high level control register (high 8 bits)
0xA2	PWM_CTRL	RW	xx00_0000b	PWM control register
0xA3	PWM_CLK_SEL	RW	xx00_0000b	PWM clock prescaler selection register
0xEF	PWM0_IO_SEL	RW	xxxx_0000b	PWM0 select IO port configuration register

11.3. PWM Register Detailed Description

PWM0_L_L (99H) PWM0 low level control register (low 4 bits)

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	PWM0_L_L[3:0]			
R/W	-	-	-	-	R/W			
Reset value	-	-	-	-	0			

PWM0_L_H (9AH) PWM0 low level control register (high 8 bits)

Bit number	7	6	5	4	3	2	1	0
Symbol	PWM0_L_H[7:0]							
R/W	R/W							
Reset value	0							

PWM0_H_L (9BH) PWM0 high level control register (low 4 bits)

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	PWM0_H_L[3:0]			
R/W	-	-	-	-	R/W			
Reset value	-	-	-	-	0			

PWM0_H_H (9CH) PWM0 high level control register (high 8 bits)

Bit number	7	6	5	4	3	2	1	0
Symbol	PWM0_H_H[7:0]							
R/W	R/W							
Reset value	0							

PWM1_L_L (9DH) PWM1 low level control register (low 4 bits)

Bit number	7	6	5	4	3	2	1	0

Symbol	-	-	-	-	PWM1_L_L[3:0]
R/W	-	-	-	-	R/W
Reset value	-	-	-	-	0

PWM1_L_H (9EH) PWM1 low level control register (high 8 bits)

Bit number	7	6	5	4	3	2	1	0
Symbol	PWM1_L_H[7:0]							
R/W	R/W							
Reset value	0							

PWM1_H_L (9FH) PWM1 high level control register (low 4 bits)

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	PWM1_H_L[3:0]			
R/W	-	-	-	-	R/W			
Reset value	-	-	-	-	0			

PWM1_H_H (A1H) PWM1 high level control register (high 8 bits)

Bit number	7	6	5	4	3	2	1	0
Symbol	PWM1_H_H[7:0]							
R/W	R/W							
Reset value	0							

PWM_EN (A2H) PWM control register

Bit number	7	6	5	4
Symbol	-	-	PWM1_CH1_ POLA_SEL	PWM1_CH0_ POLA_SEL
R/W	-	-	R/W	R/W
Reset value	-	-	0	0
Bit number	3	2	1	0
Symbol	PWM1_CH1_EN	PWM1_CH0_EN	PWM1_EN	PWM0_EN
R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0

Bit number	Bit symbol	Description
7~6	--	Reserved
5	PWM1_CH1_ POLA_SEL	PWM1_B channel polarity selection 1: The count value overflows, making the output low; 0: The count value overflows, making the output high
4	PWM1_CH0_ POLA_SEL	PWM1_A channel polarity selection 1: The count value overflows, making the output low; 0: The count value overflows, making the output high
3	PWM1_CH1_EN	PWM1_B channel enable 1: enable;

		0: Disable
2	PWM1_CH0_EN	PWM1_A channel enable 1: enable; 0: disable
1	PWM1_EN	PWM1 module enable register 1: enable; 0: disable
0	PWM0_EN	PWM0 module enable register 1: enable; 0: disable

PWM_CLK_SEL(A3H) PWM clock prescaler selection register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	PWM1_CLK_SEL			PWM0_CLK_SEL		
R/W	-	-	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	-	-	0	0	0	0	0	0

Bit number	Bit symbol	Description
7~6	--	Reserved
5~3	PWM1_CLK_SEL	PWM1 clock prescaler selection register 000: Divided by 1---24MHz 001: Divided by 2---12MHz 010: Divided by 4---6MHz 011: Divided by 6---4MHz 100: Divided by 8---3MHz 101: Divided by 12---2MHz 110: Divided by 14---1.7MHz 111: Divided by 16---1.5MHz
2~0	PWM0_CLK_SEL	PWM0 clock prescaler selection register 000: Divided by 1---24MHz 001: Divided by 2---12MHz 010: Divided by 4---6MHz 011: Divided by 6---4MHz 100: Divided by 8---3MHz 101: Divided by 12---2MHz 110: Divided by 14---1.7MHz 111: Divided by 16---1.5MHz

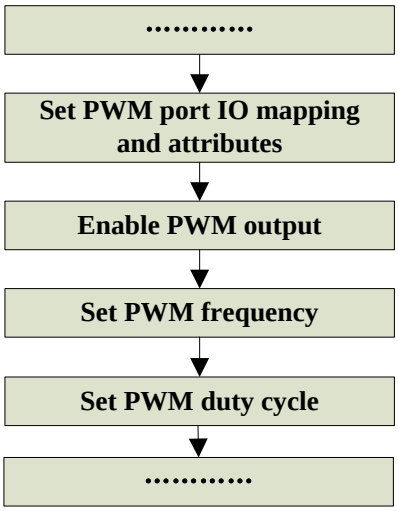
PWM0_IO_SEL (EFH) PWM0 select IO port configuration register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	PWM0_IO_SEL[3:0]			
R/W	-	-	-	-	R/W	R/W	R/W	R/W
Reset value	-	-	-	-	0	0	0	0

Bit number	Bit symbol	Description

3~0	PWM0_IO_SEL[3:0]	0: PB0 port; 1: PB1 port; 2: PB2 port; 3: PB3 port 4: PB5 port; 5: PC0 port; 6: PC3 port; 7: PC5 port; 8: PC6 port; 9: PC7 port

11.4. PWM Configure Process



PWM configure process

According to the prescaler clock selected by PWM, the recommended PWM frequency range of BF7812AMXX-XJLX series is shown in the following table:

Special frequency output of PWM: 1.7/2.3/3.0MHz, using 24MHz clock, the maximum number of stages is 14/10/8.

Prescaled clock (MHz)	Frequency Range
24	5860 Hz ~240 kHz
12	2930 Hz ~120 kHz
6	1465 Hz ~60 kHz
4	980 Hz ~40 kHz
3	735 Hz ~30 kHz
2	490 Hz ~20 kHz
1.7	420 Hz ~17 kHz
1.5	370 Hz ~15 kHz

12. Touch Key

CSD features:

- CSD charge and discharge clock three modes are optional:
  - Fixed frequency division of the system clock 6M~369k
  - PRS 1.5M normal distribution
  - PRS 1.5M evenly distribution
- CSD count clock 24M, 12M, 6M, 4M is optional;
- Counting width 9-16 bits optional;
- Support asynchronous scanning mode;
- Support wake up in idle mode 0

The BF7812AMXX-XJLX implements multiple functions through a series of register.The relationship between the capactitance detection related quantity and the SFR value is as follows:

The count value is proportional to RESO, Rb resistance, PULL_I_SELA_H, and inversely proportional to VTH_SEL. In the case of ensuring complete charge and discharge, it is proportional to the charge and discharge frequency set by PRS_DIV.

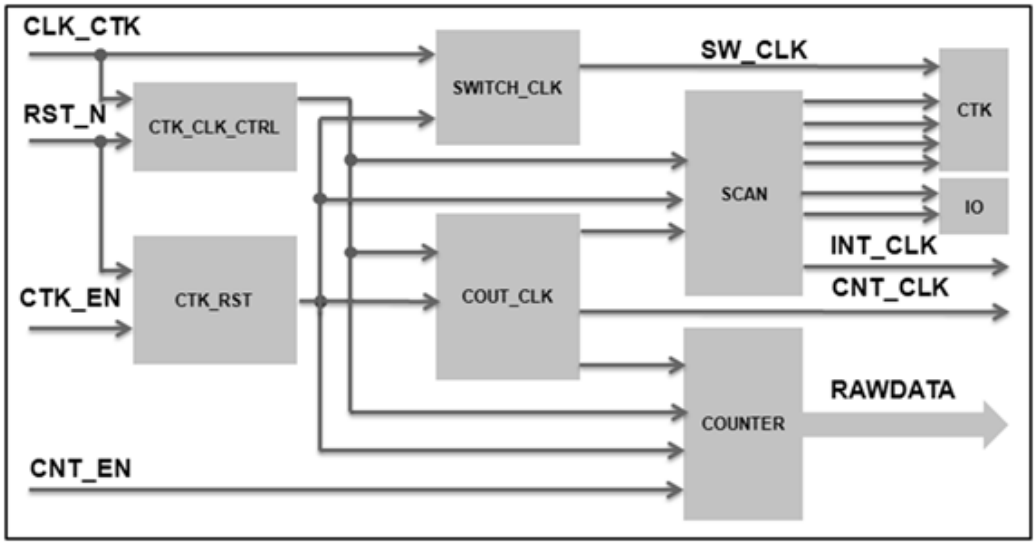
Channel touch variation is proportional to RESO and Rb, and inversely proportional to VTH_SEL. In the case of ensuring complete charge and discharge. Compared with the charge and disarge frequency set by PRS_DIV and the amount of touch change.

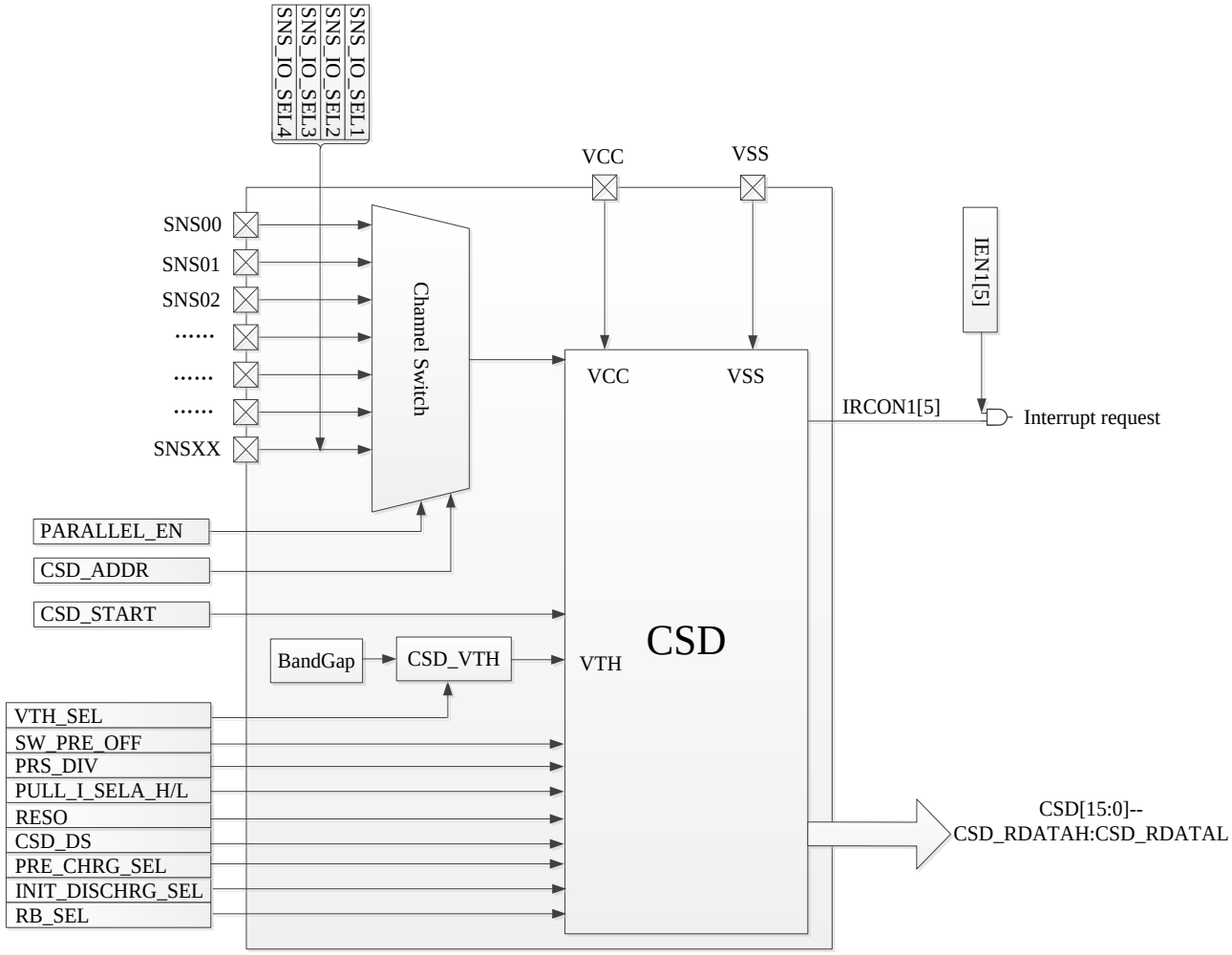
The signal-to-noise ratio of touch is proportional to VTH_SEL and PULL_I_SELA_L, and inversely proportional to CSD_DS. When the charge and discharge are incomplete, it is inversely proportional to the charge-discharge frequency set by PRS_DIV and the signal-to-noise ratio.

The time for a signal touch key detection is related to RESO and CSD_DS.

Notes: When configuring parameters, ensure that the touch key is fully charged and discharged.

CSD module structure diagram





CSD structure diagram

12.1. Touch Key Related Register

SFR register				
Address	**Name**	**RW**	**Reset value**	**Function description**
0xAA	SEL_SEN_SR_I	RW	xxxx_0000b	CSD slope control register
0xCA	CSD_START	RW	xxxx_xxx0b	CSD scan open register
0xCB	SNS_SCAN_CFG1	RW	x000_0000b	Touch key scan configuration register 1
0xCC	SNS_SCAN_CFG2	RW	x100_0000b	Touch key scan configuration register 2
0xCD	SNS_SCAN_CFG3	RW	x111_0000b	Touch key scan configuration register 3
0xCE	CSD_RAWDATAL	R	0000_0000b	CSD count value, low 8 bits
0xCF	CSD_RAWDATAH	R	0000_0000b	CSD count value, high 8 bit
0xD1	PULL_I_SELA_L	RW	0000_0000b	CSD pull up current source select register
0xD2	SNS_ANA_CFG	RW	xx10_1101b	CSD scan parameter configuration register
0xD3	SNS_IO_SEL1	RW	0000_0000b	SNS channel select register 1
0xD4	SNS_IO_SEL2	RW	0000_0000b	SNS channel select register 2
0xD5	SNS_IO_SEL3	RW	0000_0000b	SNS channel select register 3
0xD6	SNS_IO_SEL4	RW	xxxx_xx00b	SNS channel select register 4
0xE6	IEN1	RW	0000_00xxb	Interrupt enable register 1
0xF1	IRCON1	RW	0000_00xxb	Interrupt flag register 1
0xF6	IPL1	RW	0000_00xxb	Interrupt priority register 1
0xFE	PD_ANA	RW	xx00_0111b	Module switch control register

CSD registers list

12.2. Touch Key Register Detailed Description

SEL_SEN_SR_I(AAH) CSD slope control register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	-	-	-
R/W	-	-	-	-	R/W	R/W	R/W	R/W
Reset value	-	-	-	-	0	0	0	0

Bit number	Bit symbol	Description
3~0	--	CSD slope control register 1111: fast slope; Other: reserved

CSD_START(CAH) CSD scan open register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	-		-

R/W	-	-	-	-	-	-		R/W
Reset value	-	-	-	-	-	-		0

Bit number	Bit symbol	Description
0	--	1: CSD scanning is on;0: CSD scan stops Write 1 in CSD_START to start scanning. After one scan, the hardware will automatically set to 0. If you want to start the next scan, you need to set it to 1 again by software; if CSD_START=0 during the scan, the scan will stop immediately, and the module will have related internal signals Reset Note: Must be used in accordance with the process configuration: CSD_START=1, if interruption is detected, configure CSD_START=0. CSD_START is not allowed to be configured during scanning

SNS_SCAN_CFG1 (CBH) Touch key scan configuration register 1

Bit number	7	6	5	4	3	2	1	0
Symbol	-	SW_PRE_OFF	PRS_DIV					
R/W	-	R/W	R/W					
Reset value	-	0	0					

Bit number	Bit symbol	Description
6	SW_PRE_OFF	Front-end charge and discharge clock switch control. 1: close sw_clk; 0: open sw_clk
5~0	PRS_DIV	Front-end charge and discharge clock frequency selection register: 0~61: fixed frequency: F=F48M/2/(PRS_DIV+4) (6M~369K); 62: highest frequency 3M, lowest frequency 1M, center frequency 1.5M, normal distribution; 63: highest frequency 3M, lowest frequency 1M, center frequency 1.5M, evenly distributed.

SNS_SCAN_CFG2 (CCH) Touch key scan configuration register 2

Bit number	7	6	5	4	3	2	1	0
Symbol	-	PULL_I_SELA_H	PARALLEL_EN	CSD_ADDR				
R/W	-	R/W	R/W	R/W				
Reset value	-	1	0	0				

Bit number	Bit symbol	Description
6	PULL_I_SELA_H	CSD pull-up current source configuration highest bit.
5	PARALLEL_EN	SNS channel shunt enable register. 1: reserved;

		0: signal channel.
4~0	CSD_ADDR	The address of the detection channel 0~25 corresponds to the channel number 0~25

SNS_SCAN_CFG3(CDH) Touch key scan configuration register 3

Bit number	7	6	5	4	3	2	1	0
Symbol	-	RESO			CSD_DS		PRE_CHRG_SEL	INIT_DISCHRG_SEL
R/W	-	R/W			R/W		R/W	R/W
Reset value	-	1	1	1	0	0	0	0

Bit number	Bit symbol	Description
6~4	RESO	Counter bit select register. 000: 9 bits; 001: 10 bits; 010: 11 bits; 011: 12bits; 100: 13 bits; 101: 14 bits; 110: 15 bits; 111: 16 bits.
3~2	CSD_DS	Count clock frequency selection register. 00: 24M; 01: 12M; 10: 6M; 11: 4M; default 0.
1	PRE_CHRG_SEL	Pre-charge time selection 0: 20μs; 1: 40μs.
0	INIT_DISCHRG_SEL	Pre-discharge time selection 0: 2μs; 1: 10μs.

CSD_RAWDATAL (CEH) CSD counter, low 8-bit

Bit number	7	6	5	4	3	2	1	0
Symbol	CSD_RAWDATAL[7:0]							
R/W	R							
Reset value	0							

CSD_RAWDATAH (CFH) CSD counter, high 8-bit

Bit number	7	6	5	4	3	2	1	0
Symbol	CSD_RAWDATAH[7:0]							
R/W	R							
Reset value	0							

PULL_I_SELA_L (D1H) CSD pull-up current source selection register

Bit number	7	6	5	4	3	2	1	0
Symbol	PULL_I_SEL<7:0>							
R/W	R/W							
Reset value	0							

Bit number	Bit symbol	Description
7~0	PULL_I_SEL<7:0>	CSD pull up current source size selection switch. The default is 0.

SNS_ANA_CFG (D2H) CSD scan parameter configuration register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	RB_SEL			VTH_SEL		
R/W	-	-	R/W			R/W		
Reset value	-	-	1	0	1	1	0	1

Bit number	Bit symbol	Description
5~4	RB_SEL	Rb resistance size selection 100: 60k; 101: 80k; Other: reserved It is necessary to read the Rb80k calibration value from the chip Flash when using it: CBYTE[0x41CD]k/80k, to calculate the normalized sensitivity in proportion
2~1	VTH_SEL	VTH voltage selection signal 000: reserved; 001: 2.1V; 010: 2.5V; 011: 2.9V; 100: 3.2V; 101: 3.5V; 110: 3.9V; 111: 4.2V.

SNS_IO_SEL1(D3H) SNS channel select register 1

Bit number	7	6	5	4	3	2	1	0
Symbol	SNS_IO_SEL1 [7:0]							
R/W	R/W							
Reset value	0							

Bit number	Bit symbol	Description
7~0	SNS_IO_SEL1 [7:0]	SNS_IO_SEL1 [7: 0] corresponding to SNS7 ~ SNS0, the corresponding bit is 1: select SENSOR enable; 0: do not select SENSOR enable

SNS_IO_SEL2 (D4H) SNS channel select register 2

Bit number	7	6	5	4	3	2	1	0
Symbol	SNS_IO_SEL2 [7:0]							
R/W	R/W							
Reset value	0							

Bit number	Bit symbol	Description
7~0	SNS_IO_SEL2[7:0]	SNS_IO_SEL2[7:0] corresponding to SNS15 ~ SNS8, the corresponding bit is enable 1: Select SENSOR; 0: Do not select SENSOR

SNS_IO_SEL3 (D5H) SNS channel select register 3

Bit number	7	6	5	4	3	2	1	0
Symbol	SNS_IO_SEL3 [7:0]							
R/W	R/W							
Reset value	0							

Bit number	Bit symbol	Description
7~0	SNS_IO_SEL3 [7:0]	SNS_IO_SEL3 [7:0] corresponding to SNS23 ~ SNS16, the corresponding bit is enable 1: Select SENSOR; 0: Do not select SENSOR

SNS_IO_SEL4 (D6H) SNS channel select register 4

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-					SNS_IO_SEL4[1:0]	
R/W	-	-					R/W	
Reset value	-	-					0	

Bit number	Bit symbol	Description
1~0	SNS_IO_SEL4[1:0]	SNS_IO_SEL4[1:0] corresponding to SNS25~ SNS24, the corresponding bit is enable 1: Select SENSOR; 0: Do not select SENSOR

IEN1 (E6H) Interrupt enable register 1

Bit number	7	6	5	4	3	2	1	0
Symbol	EX7	EX6	EX5	EX4	EX3	EX2	-	-
R/W	R/W	R/W	R/W	R/W	R/W	R/W	-	-
Reset value	0	0	0	0	0	0	-	-

Bit number	Bit symbol	Description
5	EX5	CSD interrupt enable 1: interrupt enable; 0: interrupt disable

IRCON1 (F1H) Interrupt flag register 1

Bit number	7	6	5	4	3	2	1	0
Symbol	IE7	IE6	IE5	IE4	IE3	IE2	-	-
R/W	R/W	R/W	R/W	R/W	R/W	R/W	-	-
Reset value	0	0	0	0	0	0	-	-

Bit number	Bit symbol	Description
5	IE5	CSD interrupt flag

		1: There is a CSD interrupt flag; 0: No CSD interrupt flag

IPL1 (F6H) Interrupt priority register 1

Bit number	7	6	5	4	3	2	1	0
Symbol	IPL1.7	IPL1.6	IPL1.5	IPL1.4	IPL1.3	IPL1.2	-	-
R/W	R/W	R/W	R/W	R/W	R/W	R/W	-	-
Reset value	0	0	0	0	0	0	-	-

Bit number	Bit symbol	Description
5	IPL1.5	CSD interrupt priority. 0: low priority; 1: high priority

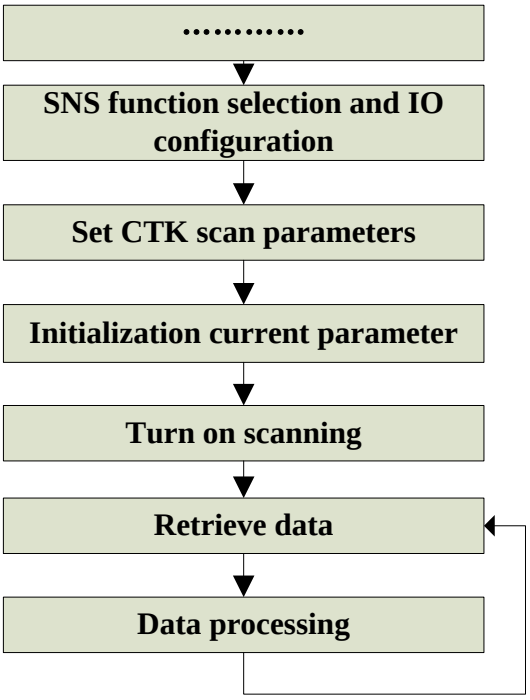
PD_ANA (FEH) Module switch control register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	LDO_LOAD2	LDO_LOAD1	XTAL_SEL	PD_XTAL	PD_CSD	PD_ADC
R/W	-	-	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	-	-	0	0	0	1	1	1

Bit number	Bit symbol	Description
1	PD_CSD	Analog CSD work control register: 0: CSD module works normally; 1: CSD module does not work

12.3. Touch Key Configure Process

CTK touch key scan for query or interrupt mode. At first, configuring the CTK scanning parameter. Second, starting CTK scanning. Then obtain and save CTK data at CTK interrupt, software algorithm for data processing and touch key output judgement.



CTK configure process

Through the sensitivity parameter configuration, a set of parameters with better signal-to-noise ratio is obtained, thereby improving the accuracy of the key judgment.

1. **RESO:** 0~7 CTK capacitiance scanning resolution, counter digits: **(RESO + 9)bit,** the bigger CTK scanning resolution, the bigger the downward rawdata, the noise is increased at the same time, conversely reverse.
2. **VTH_SEL:** 0~7, the lower VTH, the bigger raw data, the noise is increased at the same time, conversely reverse.
3. **CSD_DS:** Detect speed **0: 24M, 1: 12M, 2: 6M, 3: 4M,** the slower detect speed the slower raw data simple time, conversely reverse. Suggest default 24M, at least twice the speed of the PRS clock.
4. **RB_SEL:** Rb resistance select: **4: 60k, 5: 80k**. The greater resistance, the bigger raw data, the noise is increased at the same time, conversely reverse.
5. **PRS_DIV:** front-end charge and discharge clock frequency selection register:
   a) 0 ~61: fixed frequency: F=F48M/2/(PRS_DIV+4) (6M~369K);
   b) 62: the highest frequency 3M, the lowest frequency 1M, center frequency 1.5M, normal distribution;
   c) 63: the highest frequency 3M, the lowest frequency 1M, center frequency 1.5M, evenly distributed;
   d) The larger the PRS clock, the larger the amount of charge in Rawdata, and the greater the noise introduced, and vice versa.
6. **PULL_I_SELA_L:** pull-up current source low 8 bit.
7. **PULL_I_SELA_H:** pull-up current source high bit, default: 0x01.
   a) Current resources value =255.5-0.5*{PULL_I_SELA_H, PULL_I_SELA_L}, the smaller the current source, the smaller the count value.

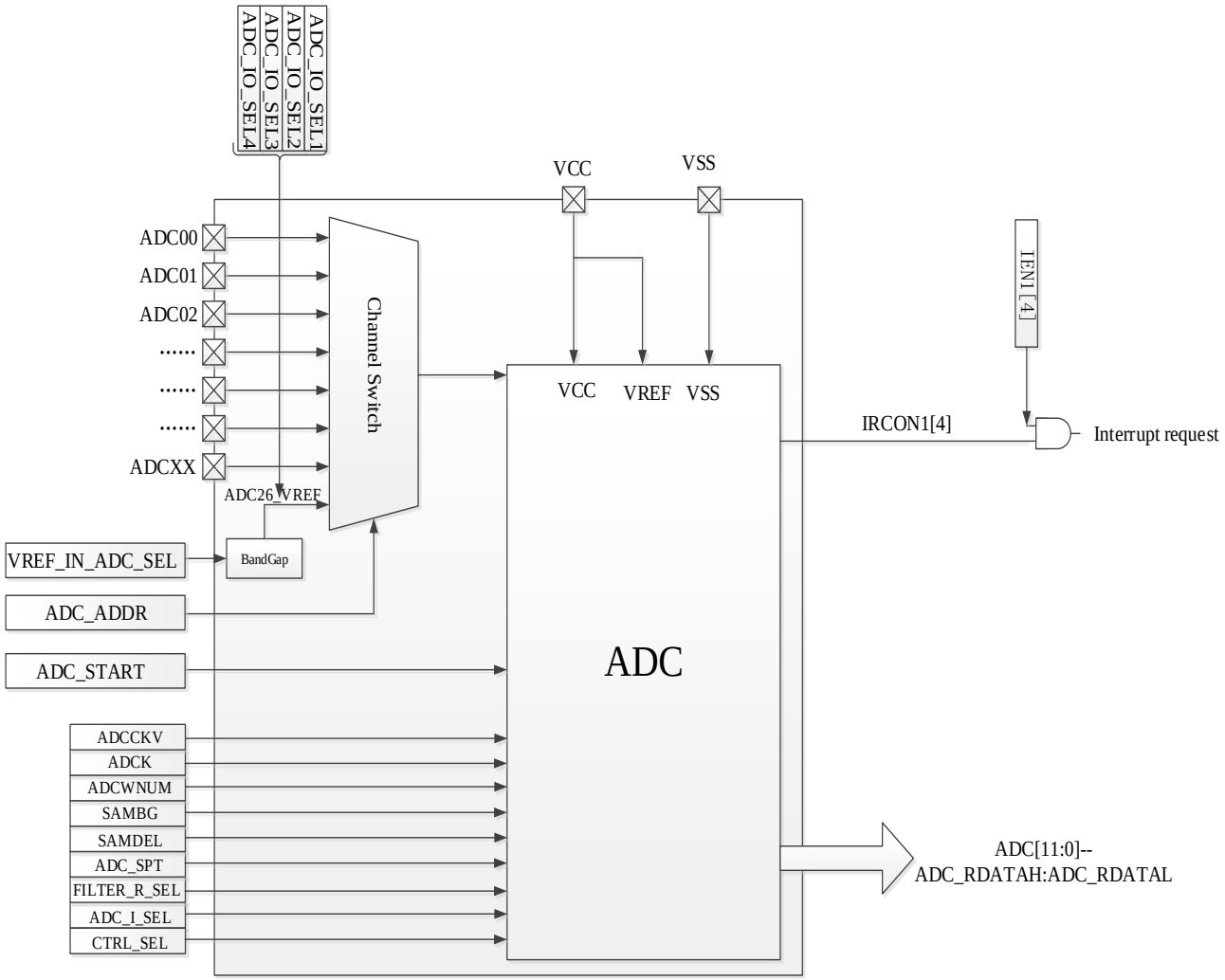
Notes:

1. **Rawdata is the real-time raw count value of the CTK capacitor counter.**
2. **In practical applications, it is necessary to view the data through the programming software and compare the parameters with good signal-to-noise ratio.**
3. **Chip supply voltage and reference voltage: VCC-VTH>0.5V.**

13. ADC

The BF7812AMXX-XJLX chip include a signal-ended, 12-bit linear successive approximation analog -to-digital converter (ADC). The reference voltage of the ADC is connected to the VCC of the chip. ADC channels can input independent analog signals. ADC module converts one channel at a time, ADC_START=0→1(⌐↑) turn on conversion. Update the ADC result register and generate an interrupt after the conversion is complete. The ADC module has the following characteristics:

- Liner successive approximation ADC with 12bit resolution;
- Single conversion mode;
- Sampling time and conversion speed are configurable;
- Support wake up in idle mode 0

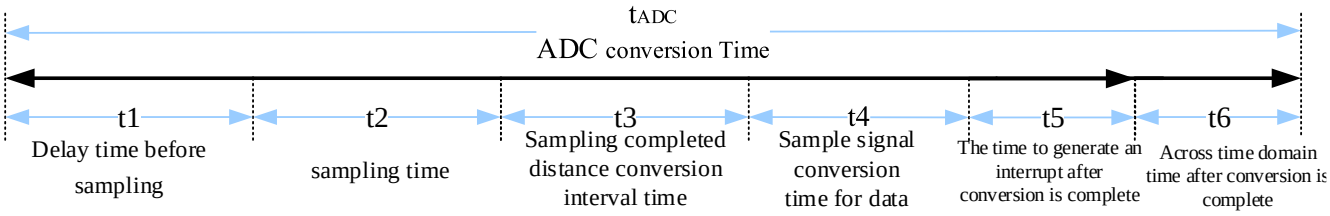


ADC block diagram

13.1. Introduction

13.1.1. ADC Conversion Time

Timing requirements: (3+ADCWNUM)/f_{ADCK} >4 /f_{ADCCKV}。
The voltage settling time after the ADC input signal is added with RC filtering is >= 2*(ADC sampling and conversion time).
ADCCKV: ADC comparator offset cancellation analog input clock (12MHz/6MHz/3MHz/2MHz optional)
ADCK: ADC clock selection (3MHz/2MHz/1.5MHz/1MHz optional)）



公式	备注
t_{ADC} = t1 + t2 + t3 + t4 + t5 +t6	ADC conversion time
t1 = SAMDEL* t_{ADCK}	SAMDEL: Pre-sampling delay time select register
t2 = 4 * (ADC_SPT+1) * t_{ADCK}	ADC_SPT: ADC sampling time configuration register
t3 = (3 + ADCWNUM) * t_{ADCK}	ADCWNUM: Distance conversion interval after sampling
t4 = 13 * t_{ADCK}	ADCK: ADC clock
t5 = 5 * t_{clk_12M} = 416.7ns	clk_12M：ADC clock source
t6 = 200ns	-

13.1.2. ADC Reference Voltage

When the power supply voltage fluctuates greatly or drops, the VCC voltage value can be inversely calculated by the formula ADCINNER_Data/ VREF_IN_ADC_SEL = 4096/VCC. The voltage value of Vin can be inversely calculated by the formula Vin_Data/Vin=4096/VCC.

ADCINNER_Data: ADC internal channel data;

Vin_Data: ADC input channel data;

Vin: input voltage;

VREF_IN_ADC_SEL: Need to read the chip calibration value, Vin = (Vin_Data/ADCINNER_Data)*VREF_IN_ADC_SEL. VREF_IN_ADC_SEL needs to read the chip calibration value, first obtain the internal channel data, and then obtain the input voltage Vin_Data data, and the time between two data acquisitions should be as short as possible;

CBYTE[0x41C4] = ADC internal channel input voltage calibration value high eight bits,

CBYTE[0x41C5] = ADC internal channel input voltage calibration value low eight bits.

Read the chip information address ADC internal channel input voltage 1.378V calibration value;

CBYTE[0x41C6] = ADC internal channel input voltage calibration value high eight bits,
CBYTE[0x41C7] = ADC internal channel input voltage calibration value low eight bits.
Read the chip information address ADC internal channel input voltage 2.271V calibration value;

CBYTE[0x41C8] = ADC internal channel input voltage calibration value high eight bits,
CBYTE[0x41C9] = ADC internal channel input voltage calibration value low eight bits.
Read the chip information address ADC internal channel input voltage 3.168V calibration value;

CBYTE[0x41CA] = ADC internal channel input voltage calibration value high eight bits,
CBYTE[0x41CB] = ADC internal channel input voltage calibration value low eight bits.
Read the chip information address ADC internal channel input voltage 4.06V calibration value;

Refer to Chapter 3 to read Flash information steps.

13.1.3. ADC Interrupt Conditions

ADC interrupt conditions: the configuration sequence is ADC_IO_SEL enable -> ADC interrupt enable -> ADC_ADDR (the address must correspond to ADC_IO_SEL) -> ADC_START. Pay attention to the initial configuration timing during application. If there is an application where the ADC and IO port functions are multiplexed, you need to pay attention to the switching timing. If the ADC_IO_SEL enable is turned off or the address does not correspond to ADC_IO_SEL, the ADC scan cannot be turned on.

13.1. ADC Related Register

SFR register				
Address	**Name**	**RW**	**Reset value**	**Function description**
0xB4	ADC_SPT	RW	0000_0000b	ADC sampling time configure register
0xB5	ADC_SCAN_CFG	RW	xx00_0000b	ADC scan control register
0xB6	ADCCKC	RW	xxxx_0000b	ADC clock control register
0xB9	ADC_RDATAH	R	xxxx_0000b	ADC scan result register, high 4 bit.
0xBA	ADC_RDATAL	R	0000_0000b	ADC scan result register lower 8 bits
0xBB	ADC_CFG1	RW	0000_0000b	ADC sampling timing control register 1
0xBC	ADC_CFG2	RW	xx00_0111b	ADC sampling timing control register 2
0xD9	ADC_IO_SEL1	RW	0000_0000b	ADC function select register 1
0xDA	ADC_IO_SEL2	RW	0000_0000b	ADC function select register 2
0xDB	ADC_IO_SEL3	RW	0000_0000b	ADC function select register 3

0xDC	ADC_IO_SEL4	RW	xxxx_xx00b	ADC function select register 4
0xE6	IEN1	RW	0000_00xxb	Interrupt enable register 1
0xF1	IRCON1	RW	0000_00xxb	Interrupt flag register 1
0xF6	IPL1	RW	0000_00xxb	Interrupt priority register 1
0xFE	PD_ANA	RW	xx00_0111b	Module switch control register

ADC registers list

13.2. ADC Register Details

ADC_SPT (B4H) ADC sample time configure register

Bit number	7	6	5	4	3	2	1	0
Symbol	ADC_SPT							
R/W	R/W							
Reset value	0							

Bit number	Bit symbol	Description
7~0	ADC_SPT	ADC sample time configure register sample time: t2 = 4 * (ADC_SPT+1) * t_{ADCK}

ADC_SCAN_CFG (B5H) ADC scan control register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	ADC_ADDR					ADC_START
R/W	-	-	R/W					R/W
Reset value	-	-	0					0

Bit number	Bit symbol	Description
5~1	ADC_ADDR	ADC channel address selection register 00000: corresponds to ADC00; 00001: corresponding to ADC01; ... 11000: corresponding to ADC24; 11001: corresponding to ADC25; 11010: corresponding to ADC26_VREF; other: reserved
0	ADC_START	ADC scan enable register 0: ADC module does not scan; 1: ADC module starts scanning ADC_START is set from 0 to 1, ADC starts to scan, after scanning once, ADC_START hardware is automatically set to 0, corresponding to the ADC interrupt flag bit, the ADC interrupt flag bit needs to be cleared by software

		Note: ADC_START is not allowed to be configured during scanning

ADCCKC (B6H) ADC clock control register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-		ADCCKV		ADCCK	
R/W	-	-	-	-	R/W		R/W	
Reset value	-	-	-	-	0	0	0	0

Bit number	Bit symbol	Description
7~4	--	Reserved
3~2	ADCCKV	ADC comparator offset cancellation analog input clock. 0: 12MHz 1: 6MHz 2: 3MHz 3: 2MHz
1~0	ADCCK	ADC clock selection. 0: 3MHz 1: 2MHz 2: 1.5MHz 3: 1MHz

ADC_RDATAH (B9H) ADC scan result register high 4 bits

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	ADC_RDATAH [3:0]			
R/W	-	-	-	-	R			
Reset value	-	-	-	-	0			

Bit number	Bit symbol	Description
3~0	ADC_RAWDATAH [3:0]	ADC scan result register

ADC_RDATAL(BAH) ADC scan result register low 8 bits

Bit number	7	6	5	4	3	2	1	0
Symbol	ADC_RDATAL[7:0]							
R/W	R							
Reset value	0							

Bit number	Bit symbol	Description
7~0	ADC_RDATAL[7:0]	ADC scan result register

ADC_CFG1(BBH) ADC sampling timing control register 1

Bit number	7	6	5	4	3	2	1	0
Symbol	ADCWNUM					SAMBG	SAMDEL	
R/W	R/W					R/W	R/W	
Reset value	0					0	0	

Bit number	Bit symbol	Description
7~3	ADCWNUM	Selection of distance conversion interval time after sampling: (3+ADCWNUM)* t_{ADCK}

2	SAMBG	Sampling timing and comparison timing interval selection 0: interval 0; 1: Interval 1* t_{ADCK}
1~0	SAMDEL	Sampling delay time selection 0: 0* t_{ADCK}; 1: 2* t_{ADCK}; 2: 4* t_{ADCK}; 3: 8* t_{ADCK}

ADC_CFG2 (BCH) ADC sampling timing control register 2

Bit number	7	6	5	4
Symbol	-	-	VREF_IN_ADC_SEL	
R/W	-	-	R/W	R/W
Reset value	-	-	0	0
Bit number	3	2	1	0
Symbol	FILTER_R_SEL	ADC_I_SEL		CTRL_SEL
R/W	R/W	R/W	R/W	R/W
Reset value	0	1	1	1

Bit number	Bit symbol	Description
5~4	VREF_IN_ADC_SEL	Input to ADC26 reference voltage selection 00: 1.378V; 01: 2.271V; 10: 3.168V; 11: 4.06V Need to read ADC internal channel input voltage calibration value when using
3	FILTER_R_SEL	Input signal filter selection 0: No RC filter added; 1: Add RC filter
2	ADC_I_SEL[1]	Op amp bias current selection signal 0: 1μA; 1: 2μA
1	ADC_I_SEL[0]	Comparator bias current selection signal 0: 1μA; 1: 2μA
0	CTRL_SEL	ADC comparator offset cancellation selection signal 00: First sampling and then offset elimination; 01: All switches are disconnected together

ADC_IO_SEL1 (D9H) ADC function selection register 1

Bit number	7	6	5	4	3	2	1	0
Symbol	ADC_IO_SEL1[7:0]							
R/W	R/W							
Reset value	0							

Bit number	Bit symbol	Description

7~0	ADC_IO_SEL1[7:0]	ADC_IO_SEL1 [7: 0] corresponding to ADC07 ~ ADC00, the corresponding bit is 1: Select ADC function; 0: Do not select ADC function

ADC_IO_SEL2(DAH) ADC function selection register 2

Bit number	7	6	5	4	3	2	1	0
Symbol	ADC_IO_SEL2[7:0]							
R/W	R/W							
Reset value	0							

Bit number	Bit symbol	Description
7~0	ADC_IO_SEL2[7:0]	ADC_IO_SEL2 [7: 0] corresponding to ADC15 ~ ADC08, the corresponding bit is 1: Select ADC function; 0: Do not select ADC function

ADC_IO_SEL3(DBH) ADC function selection register 3

Bit number	7	6	5	4	3	2	1	0
Symbol	ADC_IO_SEL3[7:0]							
R/W	R/W							
Reset value	0							

Bit number	Bit symbol	Description
7~0	ADC_IO_SEL3[7:0]	ADC_IO_SEL3 [7: 0] corresponding to ADC23 ~ ADC16, the corresponding bit is 1: Select ADC function; 0: Do not select ADC function

ADC_IO_SEL4(DCH)ADCfunction selection register 4

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	-	ADC_IO_SEL4[1:0]	
R/W	-	-	-	-	-	-	R/W	
Reset value	-	-	-	-	-	-	0	

Bit number	Bit symbol	Description
1~0	ADC_IO_SEL4[1:0]	ADC_IO_SEL4 [1: 0] corresponding to ADC25 ~ ADC24, the corresponding bit is 1: Select ADC function; 0: Do not select ADC function

IEN1 (E6H) Interrupt enable register 1

Bit number	7	6	5	4	3	2	1	0

Symbol	EX7	EX6	EX5	EX4	EX3	EX2	-	-
R/W	R/W	R/W	R/W	R/W	R/W	R/W	-	-
Reset value	0	0	0	0	0	0	-	-

Bit number	Bit symbol	Description
4	EX4	ADC interrupt enable 1: interrupt enable; 0: interrupt disable

IRCON1 (F1H) Interrupt flag register 1

Bit number	7	6	5	4	3	2	1	0
Symbol	IE7	IE6	IE5	IE4	IE3	IE2	-	-
R/W	R/W	R/W	R/W	R/W	R/W	R/W	-	-
Reset value	0	0	0	0	0	0	-	-

Bit number	Bit symbol	Description
4	IE4	ADC interrupt flag 1: There is a ADC interrupt flag; 0: No ADC interrupt flag

IPL1 (F6H) Interrupt priority register 1

Bit number	7	6	5	4	3	2	1	0
Symbol	IPL1.7	IPL1.6	IPL1.5	IPL1.4	IPL1.3	IPL1.2	-	-
R/W	R/W	R/W	R/W	R/W	R/W	R/W	-	-
Reset value	0	0	0	0	0	0	-	-

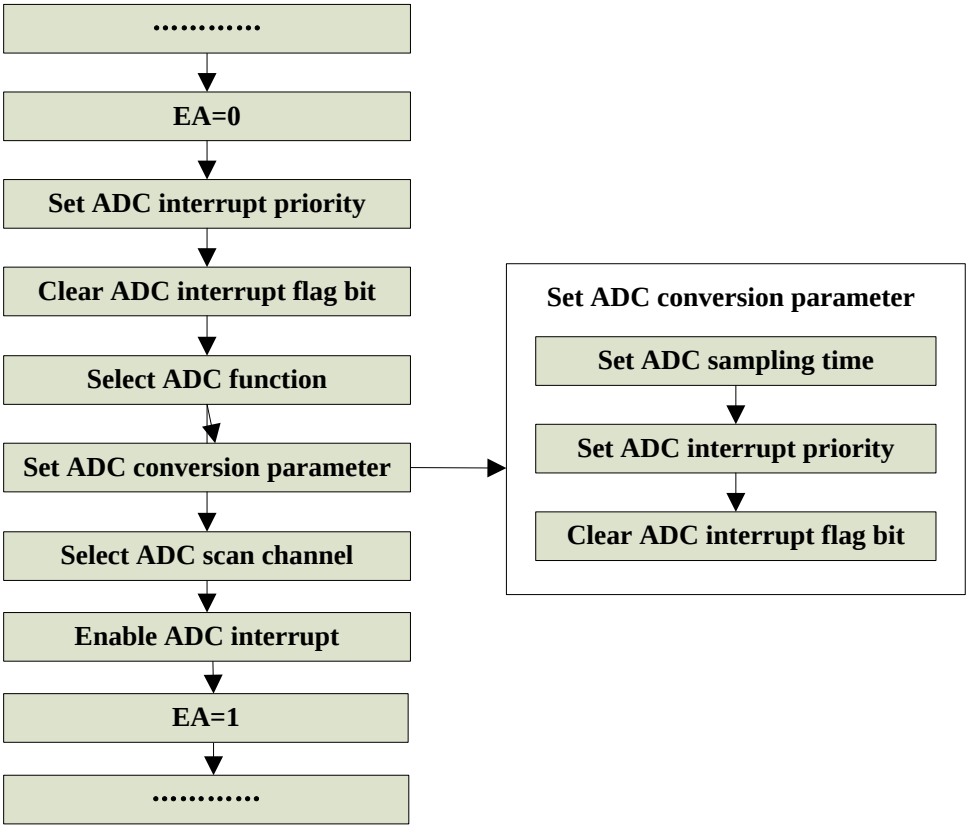
Bit number	Bit symbol	Description
4	IPL1.4	ADC interrupt priority. 0: low priority; 1: high priority

PD_ANA (FEH) Module switch control register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	LDO_LOAD2	LDO_LOAD1	XTAL_SEL	PD_XTAL	PD_CSD	PD_ADC
R/W	-	-	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	-	-	0	0	0	1	1	1

Bit number	Bit symbol	Description
0	PD_ADC	Analog ADC shutdown control register 0: ADC module works normally; 1: ADC module does not work

13.3. ADC Configuration Process



ADC configuration process

Note: When the pin is configured as ADC function, the pin needs to be configured as IO input mode, and other multiplexing functions are turned off, such as pull-up resistors, etc.

14. LVDT

The BF7812AMXX-XJLX supports low pressure alarm function, effectively monitor voltage dynamics. Support 5 levels of voltage: 3.0V/3.3V/3.6V/3.9V/4.2V (Preset point buck interrupt, hysteresis 0.1V to generate corresponding boost interrupt).

When the voltage monitoring configures the above threshold, the voltage drops to this threshold will trigger a low voltage interrupt. The system can be propely processed in low voltage interrupts according to the needs of the application.

14.1. LVDT Related Register

SFR register				
Address	**Name**	**RW**	**Reset value**	**Description**
0x86	INT_POBO_STAT	RW	xxxx_xx00b	LVDT boost/LVDT buck interrupt status register
0xE1	IRCON2	RW	xxxx_0000b	Interrupt flag register 2
0xE7	IEN2	RW	xxxx_0000b	Interrupt enable register 2
0xF4	IPL2	RW	xxxx_0000b	Interrupt priority register 2
0xFF	LVDT_SEL	RW	xxxx_1000b	LVDT control register

LVDT register list

14.2. LVDT Register Detailed Description

INT_POBO_STAT (86H) LVDT boost/LVDT buck interrupt status register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	-	INT_PO_STAT	INT_BO_STAT
R/W	-	-	-	-	-	-	R/W	R/W
Reset value	-	-	-	-	-	-	0	0

Bit number	Bit symbol	Description
1	INT_PO_STAT	Lvdt boost interrupt status 1: boost interrupt is valid 0: boost interrupt is invaild
0	INT_BO_STAT	Lvdt buck interrupt state 1: buck interrupt is valid 0: buck interrupt is invalid

IRCON2 (E1H) Interrupt flag register 2

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	IE11	IE10	IE9	IE8

R/W	-	-	-	-	R/W	R/W	R/W	R/W
Reset value	-	-	-	-	0	0	0	0

Bit number	Bit symbol	Description
0	IE8	LVDT interrupt flag 1: There is a LVDT interrupt flag; 0: No LVDT interrupt flag

IEN2(E7H) Interrupt enable register 2

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	EX11	EX10	EX9	EX8
R/W	-	-	-	-	R/W	R/W	R/W	R/W
Reset value	-	-	-	-	0	0	0	0

Bit number	Bit symbol	Description
0	EX8	LVDT interrupt enable 1: interrupt enable; 0: interrupt disable

IPL2 (F4H) Interrupt priority register 2

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	IPL2.3	IPL2.2	IPL2.1	IPL2.0
R/W	-	-	-	-	R/W	R/W	R/W	R/W
Reset value	-	-	-	-	0	0	0	0

Bit number	Bit symbol	Description
0	IPL2.0	LVDT interrupt priority. 0: low priority; 1: high priority

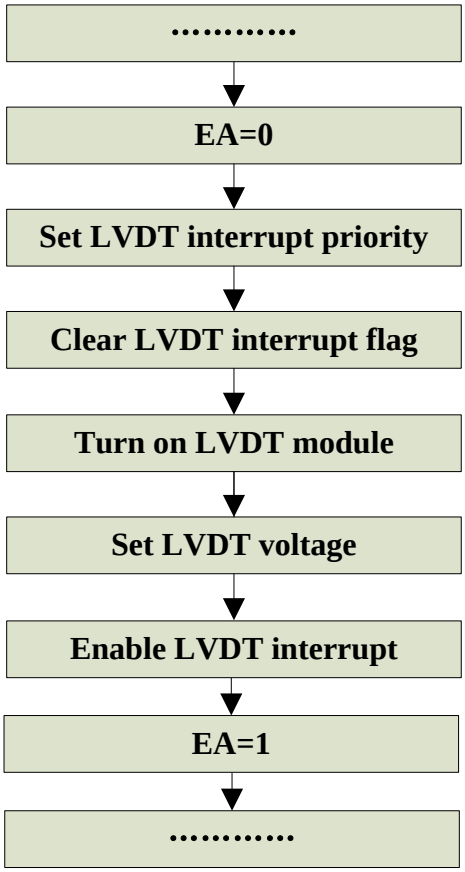
LVDT_SEL (FFH) LVDT control register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	PD_LVDT	SEL_LVDT_VTH		
R/W	-	-	-	-	R/W	R/W	R/W	R/W
Reset value	-	-	-	-	1	0	0	0

Bit number	Bit symbol	Description
3	PD_LVDT	LVDT control register 1: close; 0: open, close by default
2~0	SEL_LVDT_VTH	LVDT threshold selection 000: reserved; 001: 3.0V; 010: 3.3V; 011: 3.6V; 100: 3.9 V; others: 4.2 V;

Threshold selection SEL_LVDT_VTH	LVDT			
	Power down threshold (V)	Recovery threshold (V)	Hysteresis (mV)	Delay(μs)
001	3.0	3.1	99	6.85
010	3.3	3.4	121	7.84
011	3.6	3.7	106	8.75
100	3.9	4.0	84	9.82
other	4.2	4.3	95	10.63

14.3. LVDT Configuration Process



LVDT Configuration Process

15. LED

15.1. Function Description

Features of LED dot matrix drive mode:

- Support up to 64 LED drivers, configurable selection matrix 4x4, 4x5, 5x6, 6x7, 7x7, 7x8, 8x8;
- The scanning sequence of LED0~LED8 can be configured, n*(n-1) or (n-1)*(n-1) matrix output (n is the number of pins, n= 5~9)
- Dual lamps are turned on at the same time, the specific distribution is shown in the matrix description below;
- Single lamp on-time setting file: 8-bit register, configurable range is 16us-4.096ms, step is 16us;
- Each lamp driving time is individually selectable;
- The IO ports have multiple multiplexing relationships. Each IO port needs to be configured by software to switch to LED port. According to the LED matrix mode selection, the LED function of LED0~LED8 corresponding to the IO port is automatically turned on. The start port LED0 supports the selection of PB0~PB7, PC0, and the other ports are cycled in sequence;
- The address of the 64 lamp matrix is unique, see the matrix description below, which is used to input switch lamp information;
- Supports high current drive function of 8 GPIO ports.

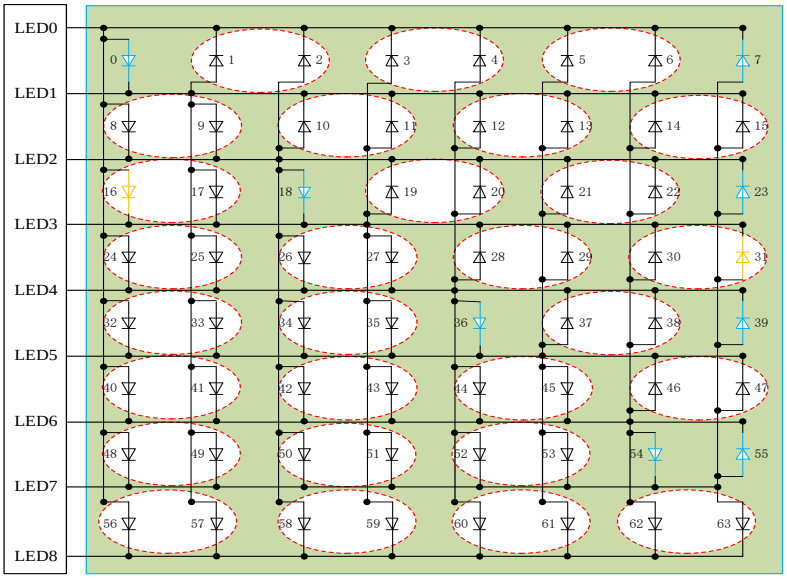
The scan mode is configurable. The software controls the LED scan to be turned on. The interrupt mode scans once interrupted and stopped. The cycle mode automatically starts to scan the next frame after the scan is completed. If there is no interruption, the software needs to turn off the scan enable.

LED dot matrix driver circuit consists of a controller, two counter, a comparator and a SRAM memory circuit.

LED dot matrix is a universal 8*8 matrix dual lamp mode scan, that is, two lights at a time (common cathode).

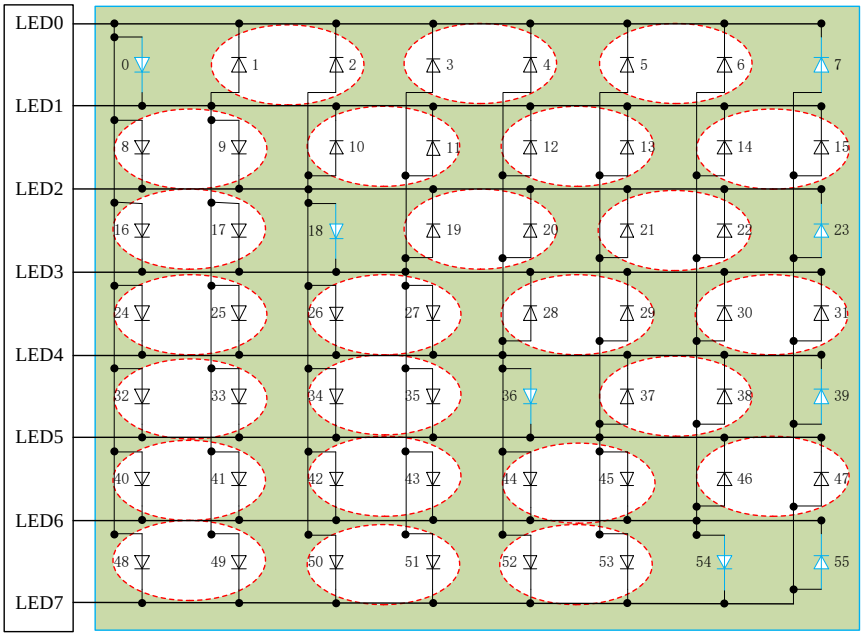
Corresponding to the LED0~LED8 port, up to 8x8=64 lights can be configured. The lights address of the corresponding position is marked in the 8*8 dot matrix below. The display configuration in the SRAM corresponding address lighting situation (1 means light, 0 means no light), The hardware code needs to resolve the lighting address and the current scanning address to automatically complete the corresponding IO port outport control. Configurable dot matrix 4x4, 4x5, 5x6, 6x7, 7x7, 7x8, 8x8, lamp addresses corresponding to different size lattices are unchanged.

8*8 matrix:



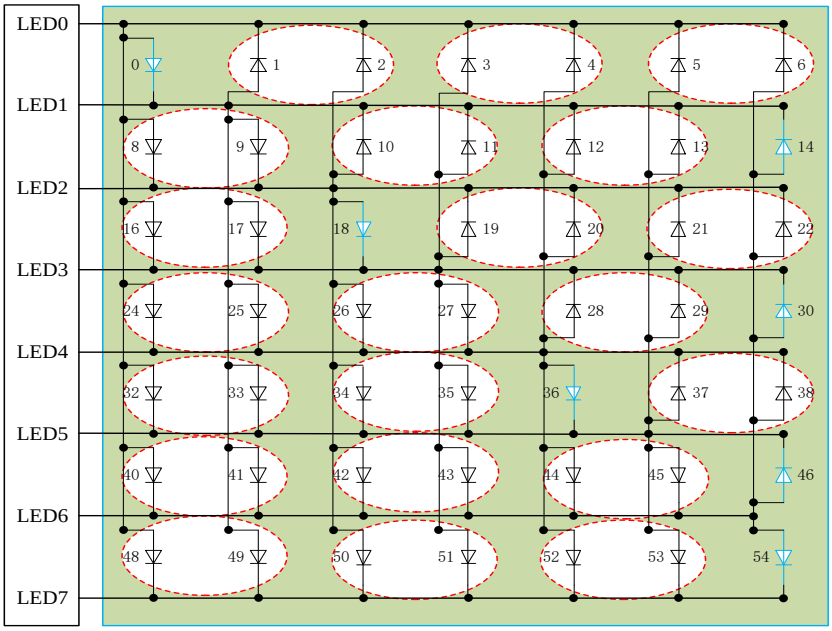
LED 8*8 matrix

7*8 matrix:



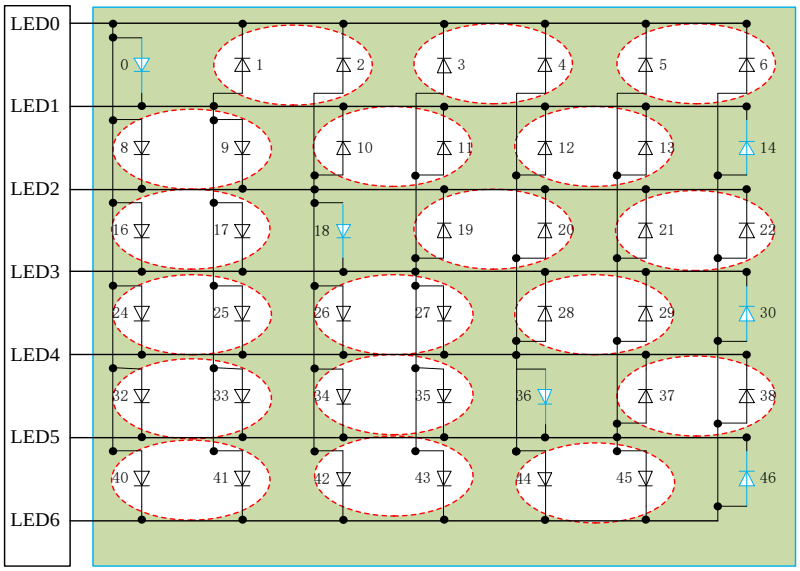
LED 7*8 matrix

7*7 lattice:



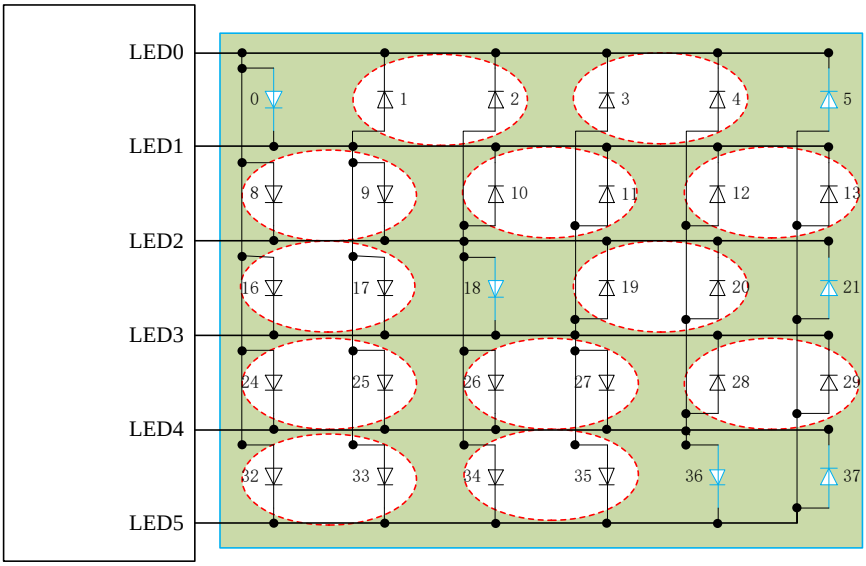
LED 7*7 matrix

6*7 matrix:



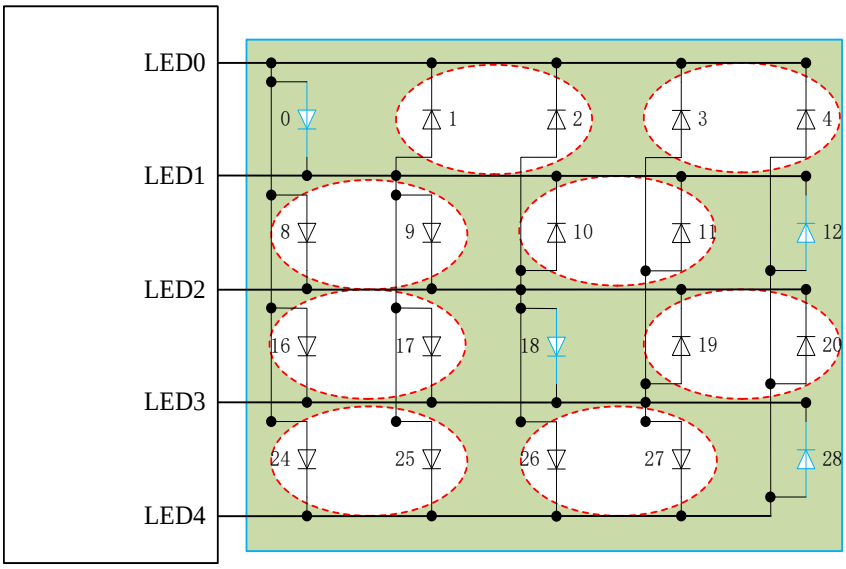
LED 6*7 matrix

5*6 matrix:



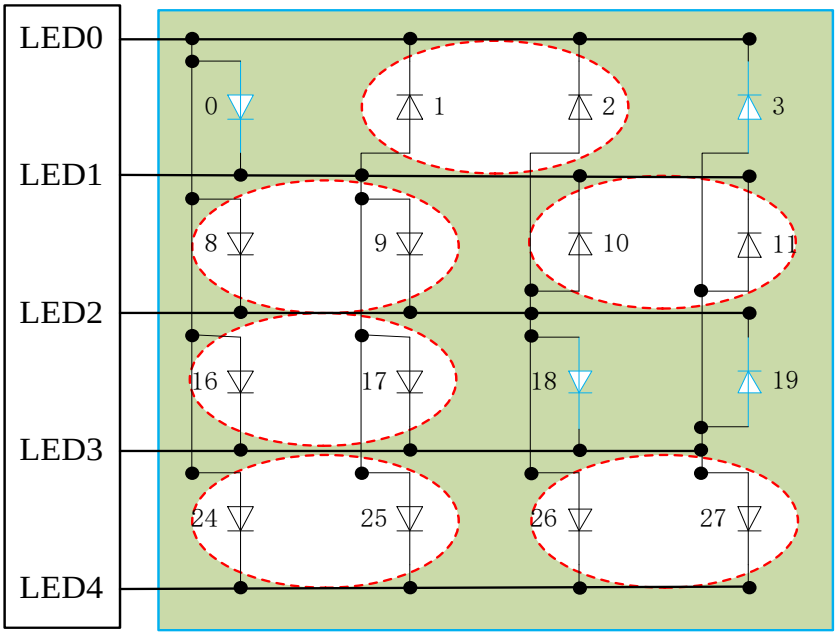
LED 5*6 matrix

4*5 matrix:



LED 4*5 matrix

4*4 matrix:

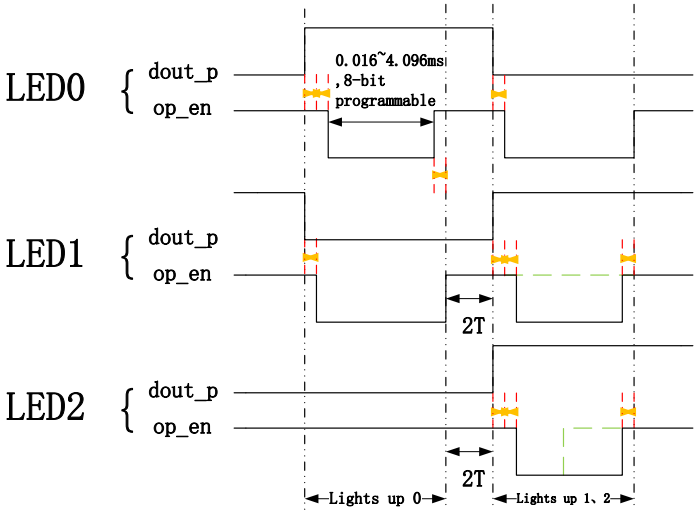


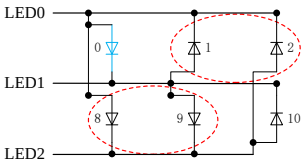
LED 4*4 matrix

Dot matrix scan timing example:

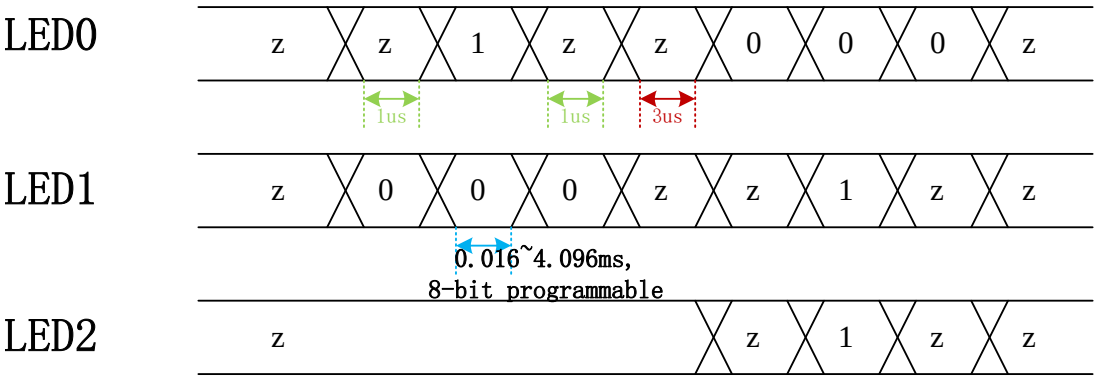
Take the lighting lamp 0, 1, 2 as an example, the timing is showen below:

- **One T，T is 1us**





The state of the IO port is as follows:



The calculation formula of the total time of led serial dot matrix is as follows:

Total scan time t = n1* $t_{\text{single led scan time}}$ + n2* $t_{\text{double led scan time}}$ + (n1+ n2)*4* t_{led}

n1: The number of single led groups.

n2: The number of double led groups.

$t_{\text{single led scan time}}$: when Dx_SEL=0, $t_{\text{single led scan time}} = t_{\text{on-time 1}}$.

when Dx_SEL=1, $t_{\text{single led scan time}} = t_{\text{on-time 2}}$.

$t_{\text{double led scan time}}$: It is determined by the long on-time. If led 1 and led 2 scan at the same time.

If led 1 on-time > led 2 on-time, $t_{\text{double led scan time}}$ = led 1 on-time.

If led 1 on-time < led 2 on-time, $t_{\text{double led scan time}}$ = led 2 on-time.

If led 1 on-time = led 2 on-time, $t_{\text{double led scan time}}$ = led 1 on-time =led 2 on-time.

t_{led}: Led clock cycle, 1us.

The on-time of each led is determined by Dx_SEL stored in sram. When Dx_SEL=0, select $t_{on\text{-}time\ 1}$; when Dx_SEL=1, select $t_{on\text{-}time\ 2}$

$t_{on\text{-}time\ 1}$: Register SCAN_WIDTH configuration;

$t_{on\text{-}time\ 2}$: Register LED2_WIDTH configuration.

15.2. LED DRIVE Current

(Ta = 25℃, VCC = 5V, LED voltage drop 2.3V)

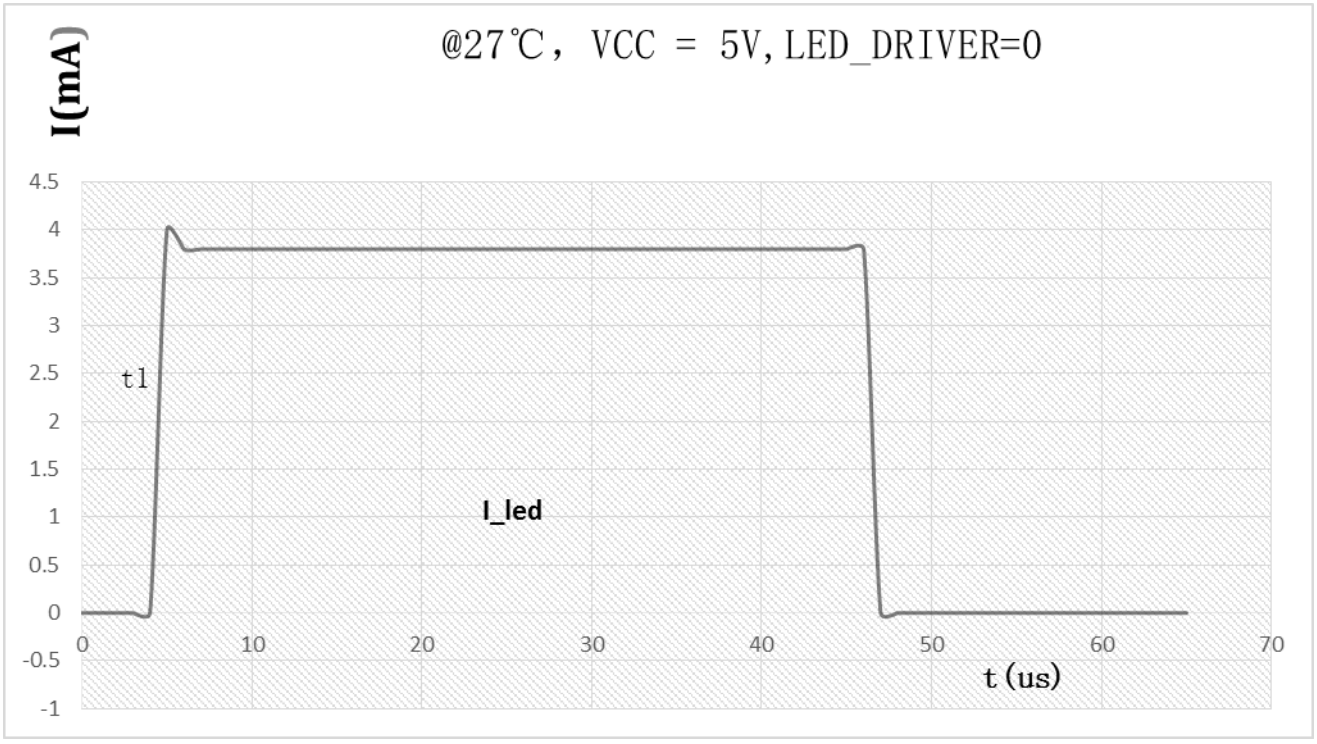
LED_DRIVE	I_led current (mA)
0	4.0
1	9.0
2	14.0
3	18.8
4	23.6
5	28.2
6	32.9
7	37.5
8	42.0
9	46.5
10	50.9
11	55.2
12	59.5
13	63.7
14	67.9
15	72.0

LED drive current register list

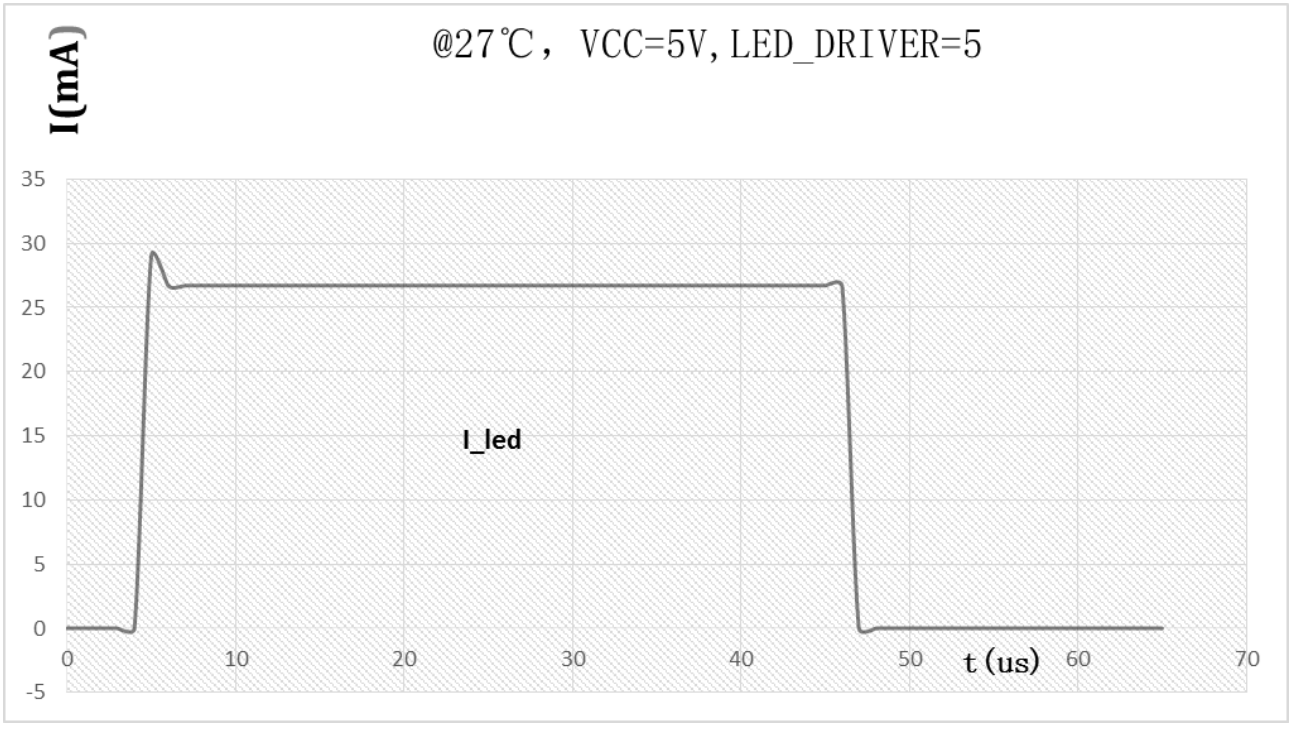
Notes:

1. **LED drive current deviation range (±8%)@VCC=5V, Ta=(-40℃~105℃), The setting of the LED_DRIVE is recommended to be smaller than the nominal Ifp of the LED lamp. The LED lamp to be driven should select the LED lamp with the same forward voltage V_F.**
2. **LED_DRIVE：LED drive capability configuration register;**
   I_led: LED lamp conducts steady state current.

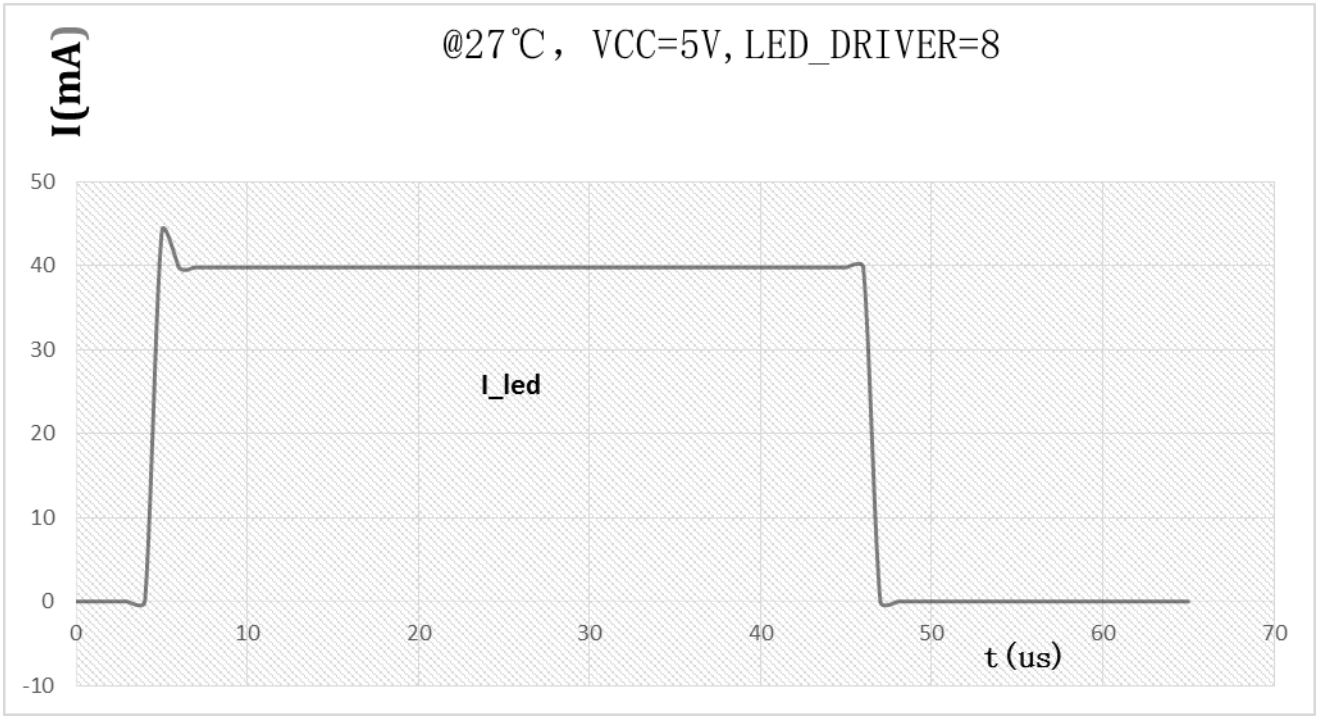
LED serial dot matrix drive current-time diagram under several common configurations:



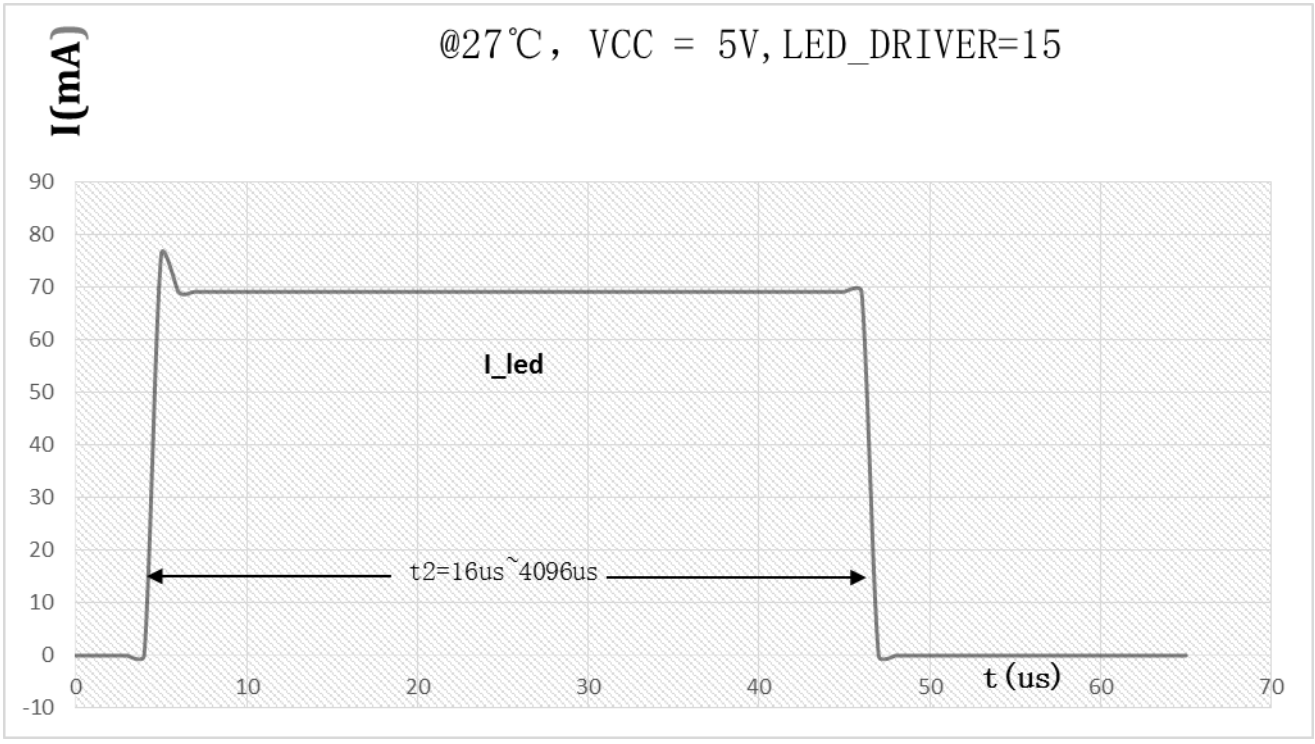
LED_DRIVER VS Time Figure1



LED_DRIVER VS Time Figure2



LED_DRIVER VS Time Figure3



LED_DRIVER VS Time Figure4

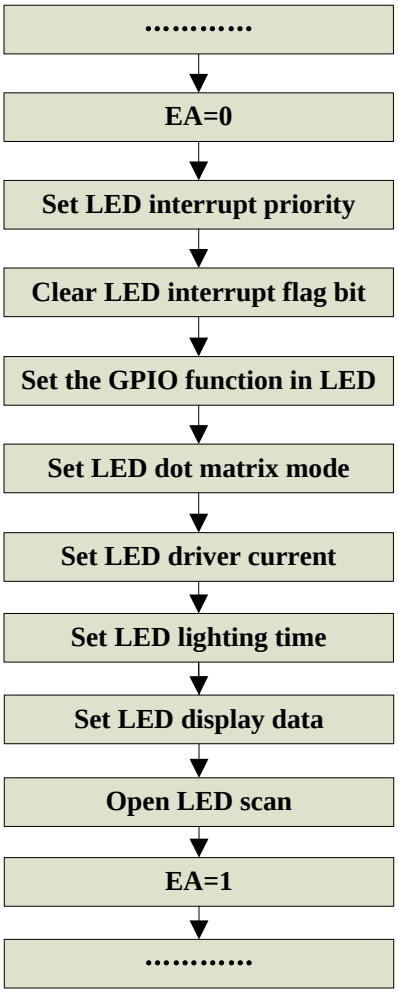
15.3. Display Configuration Address

LED dot matrix drive mode corresponding to display configuration:
Dx indicates whether the light is selected or not, 0: not bright, 1: bright;
Dx_SEL indicates that the light is selected for the lighting cycle, 0: select the first segment of the light cycle, 1: select the second segment of the light cycle.

address	7	6	5	4	3	2	1	0
200H	D7	D6	D5	D4	D3	D2	D1	D0
201H	D15	D14	D13	D12	D11	D10	D9	D8
202H	D23	D22	D21	D20	D19	D18	D17	D16
203H	D31	D30	D29	D28	D27	D26	D25	D24
204H	D39	D38	D37	D36	D35	D34	D33	D32
205H	D47	D46	D45	D44	D43	D42	D41	D40
206H	D55	D54	D53	D52	D51	D50	D49	D48
207H	D63	D62	D61	D60	D59	D58	D57	D56
208H	D7_SEL	D6_SEL	D5_SEL	D4_SEL	D3_SEL	D2_SEL	D1_SEL	D0_SEL
209H	D15_SEL	D14_SEL	D13_SEL	D12_SEL	D11_SEL	D10_SEL	D9_SEL	D8_SEL
20AH	D23_SEL	D22_SEL	D21_SEL	D20_SEL	D19_SEL	D18_SEL	D17_SEL	D16_SEL
20BH	D31_SEL	D30_SEL	D29_SEL	D28_SEL	D27_SEL	D26_SEL	D25_SEL	D24_SEL
20CH	D39_SEL	D38_SEL	D37_SEL	D36_SEL	D35_SEL	D34_SEL	D33_SEL	D32_SEL
20DH	D47_SEL	D46_SEL	D45_SEL	D44_SEL	D43_SEL	D42_SEL	D41_SEL	D40_SEL
20EH	D55_SEL	D54_SEL	D53_SEL	D52_SEL	D51_SEL	D50_SEL	D49_SEL	D48_SEL
20FH	D63_SEL	D62_SEL	D61_SEL	D60_SEL	D59_SEL	D58_SEL	D57_SEL	D56_SEL

LED dot matrix drive mode table

15.4. LED Configure Process



LED configure process

15.5. LED Related Register

SFR register				
Address	**Name**	**RW**	**Reset Value**	**Function description**
0xAB	LED_IO_START	RW	xxxx_0000b	LED port matrix start PAD selection register
0xAF	SCAN_START	RW	xxxx_xxx0b	LED scan open register
0xB0	DP_CON	RW	xxx0_0000b	LED scan control register
0xB1	SCAN_WIDTH	RW	0000_0000b	LED scan on time 1 control register
0xB2	LED2_WIDTH	RW	0000_0000b	LED scan on time 2 control register
0xB3	LED_DRIVE	RW	xxxx_0000b	LED drive capability configuration register
0xC2	COM_IO_SEL	RW	0000_0000b	COM selection configuration register
0xE6	IEN1	RW	0000_00xxb	Interrupt enable register 1
0xF1	IRCON1	RW	0000_00xxb	Interrupt flag register 1
0xF6	IPL1	RW	0000_00xxb	Interrupt priority register 1

LED registers list

15.6. LED Register Detailed Description

LED_IO_START(ABH) LED port matrix start PAD selection register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	-	-	-
R/W	-	-	-	-	R/W	R/W	R/W	R/W
Reset value	-	-	-	-	0	0	0	0

Bit number	Bit symbol	Description
3~0	--	LED port matrix start PAD selection register 0000: PB0 port; 0001: PB1 port; 0010: PB2 port; 0011: PB3 port; 0100: PB4 port; 0101: PB5 port; 0110: PB6 port; 0111: PB7 port; 1000: PC0 port; Other: PB0 port The starting port LED0 selects the specific position of the PAD, and the remaining LEDX are arranged in order from top to bottom, and if PC0 is exceeded, they are arranged in cyclic order from PB0. For example: LED_IO_START=0111, DUTY_SEL=7, then LED0: PB7, LED1: PC0, LED2: PB0, LED3: PB1, LED4: PB2, LED5: PB3, LED6: PB4, LED7: PB5, LED8: PB6

SCAN_START(AFH) LED scan open register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	-	-	-
R/W	-	-	-	-	-	-	-	R/W
Reset value	-	-	-	-	-	-	-	0

Bit number	Bit symbol	Description
0	--	LED scan on register 1: Scan on; 0: Scan off

DP_CON (B0H) LED scan control register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	DUTY_SEL			SCAN_MODE	COM_MOD
R/W	-	-	-	R/W			R/W	R/W
Reset value	-	-	-	0	0	0	0	0

Bit number	Bit symbol	Description
4~2	DUTY_SEL	LED port drive mode matrix selection configuration register 0: no matrix; 1: 4x4 matrix; 2: 4x5 matrix; 3: 5x6 matrix; 4: 6x7 matrix; 5: 7x7 matrix; 6: 7x8 matrix; 7: 8x8 matrix
1	SCAN_MODE	LED scan mode. 1: cycle scan mode 0: interrupt scan mode
0	COM_MOD	Large sink current ports drive enable. 1: COM port function lock, work as a large current IO port. 0: COM port function is not locked and can be configured as other functions. When the COM port locks the large sink current IO port, by configuring GPIO registers output drive timing, it is vaild when all of the following LED scan configurations are invalid.

SCAN_WIDTH (B1H) LED scan on time 1 control register

Bit number	7	6	5	4	3	2	1	0
Symbol	-							
R/W	R/W							

Reset value	0

Bit number	Bit symbol	Description
7~0	--	In the LED dot matrix drive mode, the corresponding single lamp lighting time configuration register-the first segment of lamp cycle configuration period=(scan_width+1)*16us, support configuration range 0.016~4.096ms

LED2_WIDTH (B2H) LED scan on time 2 control register

Bit number	7	6	5	4	3	2	1	0
Symbol	-							
R/W	R/W							
Reset value	0							

Bit number	Bit symbol	Description
7~0	--	In the LED dot matrix drive mode, the corresponding single lamp lighting time configuration register-the second stage of lamp cycle configuration period=(led2_width+1)*16us, support configuration range 0.016~4.096ms

LED2_DRIVE (B3H) LED drive capability configuration register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-			
R/W	-	-	-	-	R/W			
Reset value	-	-	-	-	0			

Bit number	Bit symbol	Description
3~0	-	LED port drive capability configuration register 0~15------4mA~72mA, please refer to LED drive ammeter for details.

COM_IO_SEL (C2H) COM port selection configuration register

Bit number	7	6	5	4	3	2	1	0
Symbol	COM7	COM6	COM5	COM4	COM3	COM2	COM1	COM0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Bit number	Bit symbol	Description
7~0	--	COM port selection configuration register, corresponding to PB port

		1: Select COM port mode; 0: select IO port mode

IEN1 (E6H) Interrupt enable register 1

Bit number	7	6	5	4	3	2	1	0
Symbol	EX7	EX6	EX5	EX4	EX3	EX2	-	-
R/W	R/W	R/W	R/W	R/W	R/W	R/W	-	-
Reset value	0	0	0	0	0	0	-	-

Bit number	Bit symbol	Description
6	EX6	LED interrupt enable 1: interrupt enable; 0: interrupt disable

IRCON1 (F1H) Interrupt flag register 1

Bit number	7	6	5	4	3	2	1	0
Symbol	IE7	IE6	IE5	IE4	IE3	IE2	-	-
R/W	R/W	R/W	R/W	R/W	R/W	R/W	-	-
Reset value	0	0	0	0	0	0	-	-

Bit number	Bit symbol	Description
6	IE6	LED interrupt flag 1: There is a LED interrupt flag; 0: No LED interrupt flag

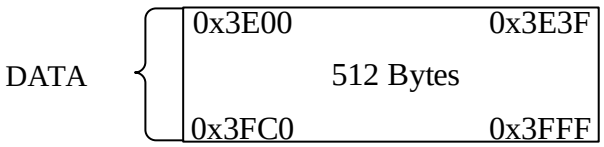
IPL1 (F6H) Interrupt priority register 1

Bit number	7	6	5	4	3	2	1	0
Symbol	IPL1.7	IPL1.6	IPL1.5	IPL1.4	IPL1.3	IPL1.2	-	-
R/W	R/W	R/W	R/W	R/W	R/W	R/W	-	-
Reset value	0	0	0	0	0	0	-	-

Bit number	Bit symbol	Description
6	IPL1.6	LED interrupt priority. 0: low priority; 1: high priority

16. DATA

The size of the DATA area is 512 Bytes for one page, and the address is (0x3E00~0x3FFF). When using, it needs to be page erased, and then the byte write operation can be performed. After erasing, it can only be written once.



When SPROG_ADDR_H[1] = 0,

{SPROG_ADDR_H[0], SPROG_ADDR_L[7:0]}, the logical address (0~511) corresponds to the physical address (0x3E00~0x3FFF).

16.1. Page Erase Step

1. SPROG_TIM[4:0] = 0~20 (30ms recommended), the byte write time is fixed at 62 μs, and it is only configured once in the main program main() function initialization;
2. Turn off the interrupt;
3. Configure SPROG_ADDR_L = 0x00;
4. Configure SPROG_ADDR_H = 0x00, erase this page;
5. Configure SPROG_CMD = 0x96;
6. Write 4 NOP instructions;
7. Start erasing, the CPU turns off the clock f_{SYS}, and turns on the clock f_{SYS} after erasing is completed;
8. Need to continue to erase data, skip to step 3;
9. Configure SPROG_ADDR_H=0x00 and SPROG_ADDR_L=0x00 to restore interrupt settings.

16.2. Byte Write Step

1. SPROG_TIM[4:0] = 0~20 (30 ms recommended), the byte write time is fixed at 62 μs, and it is only configured once in the main program main() function initialization;
2. Turn off the interrupt;
3. Configure SPROG_ADDR_L, SPROG_ADDR_H, select the address of the programming byte;
4. Configure SPROG_DATA;
5. Configure SPROG_CMD = 0x69;
6. Write 4 NOP instructions;
7. Start writing, the CPU turns off the clock f_{SYS}, and turns on the clock f_{SYS} after completion;
8. Need to continue programming data, skip to step 3;
9. Configure SPROG_ADDR_H=0x00 and SPROG_ADDR_L=0x00 to restore interrupt settings.

16.3. Registers

SFR register				
Address	**Name**	**RW**	**Reset value**	**Function description**
0xF9	SPROG_ADDR_H	RW	xx00_0000b	Address control register
0xFA	SPROG_ADDR_L	RW	0000_0000b	Address control register lower 8 bits
0xFB	SPROG_DATA	RW	0000_0000b	Data register
0xFC	SPROG_CMD	RW	0000_0000b	Command register
0xFD	SPROG_TIM	RW	xxx0_1010b	Erase and write time control register

16.3.1. Address Control Register

SPROG_ADDR_H (F9H) Address control register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	-	-	-
R/W	-	-	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	-	-	0	0	0	0	0	0

Bit number	Bit symbol	Description
5~0	--	In non-FLASH BOOT upgrade mode, Bit[1:0] of this register is valid: Bit[1]: 0: select DATA area; 1: reserved; Bit[0]: High bit of the DATA area address, { SPROG_ADDR_H[0], SPROG_ADDR_L[7:0]} constitute the DATA area address In FLASH BOOT upgrade mode, Bit[5:0] of this register is valid: {SPROG_ADDR_H[5:0], SPROG_ADDR_L[7:0]} are multiplexed to address all spaces of CODE from 0x0000~0x3FFF

16.3.2. Address Control Register Lower 8 Bits

SPROG_ADDR_L(FAH) Address control register lower 8 bits

Bit number	7	6	5	4	3	2	1	0
Symbol	SPROG_ADDR_L[7:0]							
R/W	R/W							
Reset value	0							

Bit number	Bit symbol	Description
7~0	SPROG_ADDR_L[7:0]	lower 8 bits of address

16.3.4. Data Register

SPROG_DATA(FBH) Data register

Bit number	7	6	5	4	3	2	1	0
Symbol	-							
R/W	R/W							
Reset value	0							

Bit number	Bit symbol	Description
7~0	--	data to be written

16.3.5. Command Register

SPROG_CMD(FCH) Command register

Bit number	7	6	5	4	3	2	1	0
Symbol	-							
R/W	R/W							
Reset value	0							

Bit number	Bit symbol	Description
7~0	--	Write 0x96: page erase; Write 0x69: byte programming When continuously writing data 0x12, 0x34, 0x56, 0x78, 0x9a, enter the BOOT upgrade mode of Flash; When writing data 0xfe, 0xdc, 0xba, 0x98, 0x76 continuously, exit the BOOT upgrade mode of Flash; When CFG_BOOT_EN=1 or the program is running in a non-BOOT space, the BOOT upgrade mode cannot be entered

16.3.6. Erase and Write Time Control Register

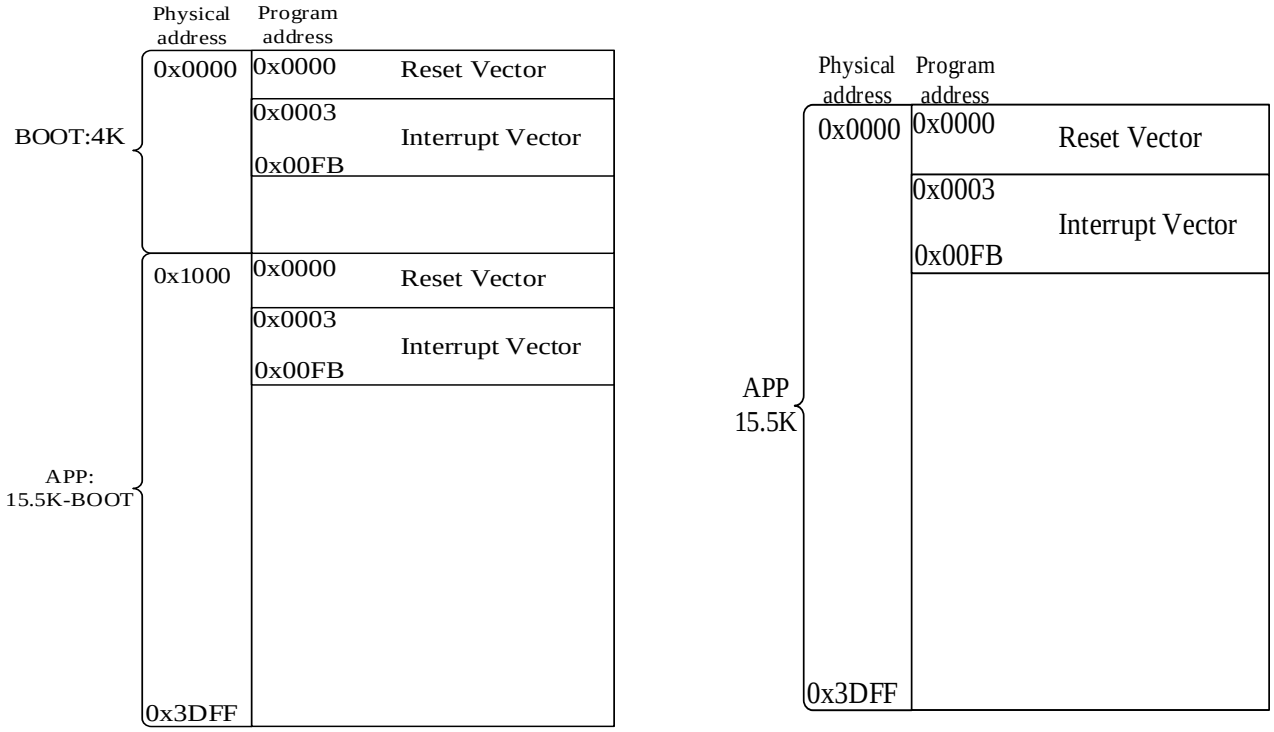
SPROG_TIM (FDH) Erase and write time control register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	-	-	-
R/W	-	-	-	R/W	R/W	R/W	R/W	R/W
Reset value	-	-	-	1	1	0	1	0

Bit number	Bit symbol	Description
7~5	--	reserved
4~0	--	Byte write fixed time 62μs 0~20: erasing time=20 + SPROG_TIM[4:0] (ms); >20: Erase time=30ms

17. IAP Operation

Flash supports the IAP BOOT upgrade function, and realizes the jump between the BOOT area and the APP area by sending IAP operation commands. The BOOT has its own storage and write protection, and the size of the BOOT area is 4K.



Left: BOOT and APP partition map; Right: APP area without BOOT map

17.1. Flash IAP Related Registers

SFR register				
Address	**Name**	**RW**	**Reset value**	**Description**
0xF9	SPROG_ADDR_H	RW	xx00_0000b	Address control register
0xFA	SPROG_ADDR_L	RW	0000_0000b	Address control register lower 8 bits
0xFB	SPROG_DATA	RW	0000_0000b	Data register
0xFC	SPROG_CMD	RW	0000_0000b	Command register
0xFD	SPROG_TIM	RW	xxx0_1010b	Erase and write time control register

Flash IAP registers list

Secondary bus register				
Address	**Name**	**RW**	**Reset value**	**Description**
0x21	FLASH_BOOT_EN	R	xxxx_xxx0b	BOOT mode status register
0x22	BOOT_CMD	RW	0000_0000b	Program space jump instruction register
0x23	ROM_OFFSET_L	R	0000_0000b	Address offset of CODE area (low 8 bits)
0x24	ROM_OFFSET_H	R	0000_0000b	Address offset of CODE area (high 8 bits)

Flash IAP secondary bus registers list

17.2. Flash IAP Register Detailed Description

SPROG_ADDR_H (F9H) Address control register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	-	-	-
R/W	-	-	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	-	-	0	0	0	0	0	0

Bit number	Bit symbol	Description
5~0	--	In non-FLASH BOOT upgrade mode, Bit[1:0] of this register is valid: Bit[1]: 0: select DATA area, 1: reserved; Bit[0]: High bit of the DATA area address, { SPROG_ADDR_H[0], SPROG_ADDR_L[7:0]} constitute the DATA area address In FLASH BOOT upgrade mode, Bit[5:0] of this register is valid: {SPROG_ADDR_H[5:0], SPROG_ADDR_L[7:0]} are multiplexed to address all spaces of CODE from 0x0000~0x3FFF

SPROG_ADDR_L(FAH) Address control register lower 8 bits

Bit number	7	6	5	4	3	2	1	0
Symbol	SPROG_ADDR_L[7:0]							
R/W	R/W							
Reset value	0							

Bit number	Bit symbol	Description
7~0	SPROG_ADDR_L[7:0]	lower 8 bits of address

SPROG_DATA(FBH) Data register

Bit number	7	6	5	4	3	2	1	0
Symbol	-							
R/W	R/W							
Reset value	0							

Bit number	Bit symbol	Description
7~0	--	data to be written

SPROG_CMD(FCH) Command register

Bit number	7	6	5	4	3	2	1	0
Symbol	-							
R/W	R/W							
Reset value	0							

Bit number	Bit symbol	Description
7~0	--	Write 0x96: page erase; Write 0x69: byte programming When continuously writing data 0x12, 0x34, 0x56, 0x78, 0x9a, enter the BOOT upgrade mode of Flash; When writing data 0xfe, 0xdc, 0xba, 0x98, 0x76 continuously, exit the BOOT upgrade mode of Flash; When CFG_BOOT_EN=1 or the program is running in a non-BOOT space, the BOOT upgrade mode cannot be entered

SPROG_TIM (FDH) Erase and write time control register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	-	-	-
R/W	-	-	-	R/W	R/W	R/W	R/W	R/W
Reset value	-	-	-	1	1	0	1	0

Bit number	Bit symbol	Description
7~5	--	reserved

4~0	--	Byte write fixed time 62μs 0~20: erasing time=20 ms ~40ms (step 1ms); >20: Erase time=30ms

Secondary bus register:

FLASH_BOOT_EN (21H) BOOT mode status register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	-	-	FLASH_BOOT_EN
R/W	-	-	-	-	-	-	-	R
Reset value	-	-	-	-	-	-	-	0

Bit number	Bit symbol	Description
0	FLASH_BOOT_EN	1: Enter Flash BOOT upgrade mode, 0: Exit Flash BOOT upgrade mode. Note: In this mode, SPROG_ADDR_H, SPROG_ADDR_L, SPROG_DATA, SPROG_CMD, SPROG_TIM are reused as the BOOT upgrade function. {SPROG_ADDR_H, SPROG_ADDR_L} are multiplexed into all Flash space addresses from 0x0000 to 0x7FFF.

BOOT_CMD (22H) Program space jump instruction register

Bit number	7	6	5	4	3	2	1	0
Symbol	-							
R/W	RW							
Reset value	0							

Bit number	Bit symbol	Description
7~0	--	Configure the program space jump instruction, write 5 groups of data (0xFF, 0x00, 0x88, 0x55, 0xAA) continuously, and jump into the main program space; Continuously write 5 groups of data (0x37, 0xC8, 0x42, 0x9A, 0x65), jump into the Boot program space; the value read out is the most recently written byte.

ROM_OFFSET_L (23H) Address offset of CODE area (low 8 bits)

Bit number	7	6	5	4	3	2	1	0
Symbol	-							
R/W	RO							
Reset value	0							

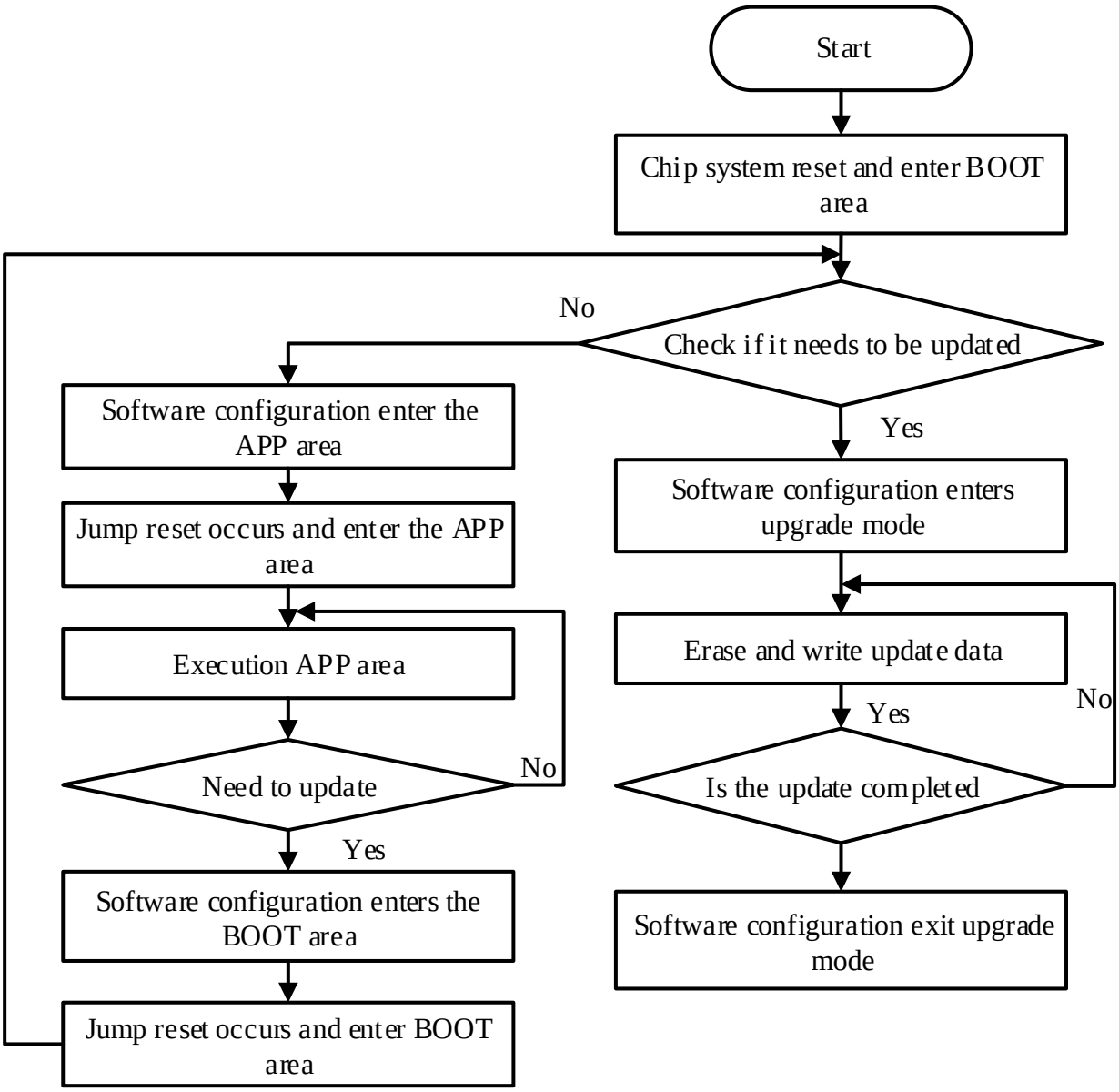
Bit number	Bit symbol	Description
7~0	--	Address offset of CODE area (low 8 bits)

ROM_OFFSET_H (24H) Address offset of CODE area (high 8 bits)

Bit number	7	6	5	4	3	2	1	0
Symbol	-							
R/W	RO							
Reset value	0							

Bit number	Bit symbol	Description
7~0	--	Address offset of CODE area (high 8 bits)

17.3. Flash IAP Operation Process



17.3.1. Flash IAP Erase Step

In Flash_BOOT upgrade mode:

1. SPROG_TIM[4:0] = 0~20 (30 ms recommended), the byte write time is fixed at 62 us, and it is only configured once in the main program main() function initialization;
2. Turn off the interrupt;
3. Configure SPROG_ADDR_L = 0x00;
4. Configure SPROG_ADDR_H[5:1] and choose to erase the page;
5. Configure SPROG_CMD = 0x96;
6. Write 4 NOP instructions;
7. Start erasing, the CPU turns off the clock f_{SYS}, and turns on the clock f_{SYS} after erasing is completed;
8. Need to continue to erase data, skip to step 2;
9. Configure SPROG_ADDR_H=0x00 and SPROG_ADDR_L=0x00 to restore interrupt settings.

17.3.2. Flash IAP Byte Write Step

In Flash_BOOT upgrade mode:

1. SPROG_TIM[4:0] = 0~20 (30 ms recommended), the byte write time is fixed at 62 us, and it is only configured once in the main program main() function initialization;
2. Turn off the interrupt;
3. Configure SPROG_ADDR_L, SPROG_ADDR_H, select the address of the programming byte;
4. Configure SPROG_DATA;
5. Configure SPROG_CMD = 0x69;
6. Write 4 NOP instructions;
7. Start writing, the CPU turns off the clock f_{SYS}, and turns on the clock f_{SYS} after completion;
8. Need to continue programming data, skip to step 2;
9. Configure SPROG_ADDR_H=0x00 and SPROG_ADDR_L=0x00 to restore interrupt settings.

17.3.3. Flash IAP Operation Instruction

Instruction	Instruction response status	Instruction data
Enter upgrade mode instruction	FLASH_BOOT_EN = 1	0x12, 0x34, 0x56, 0x78, 0x9A
Exit upgrade mode instruction	FLASH_BOOT_EN = 0	0xFE, 0xDC, 0xBA, 0x98, 0x76
Enter the APP area instruction	ROM_OFFSETH/L	0xFF, 0x00, 0x88, 0x55, 0xAA
Enter the BOOT area instruction	ROM_OFFSETH/L	0x37, 0xC8, 0x42, 0x9A, 0x65

Instructions for operation:

1. Enter upgrade mode instruction: SPROG_CMD sequential write: 0x12, 0x34, 0x56, 0x78, 0x9A;
2. Exit upgrade mode instruction: SPROG_CMD sequential write: 0xFE, 0xDC, 0xBA, 0x98, 0x76;
3. Enter the APP area instruction: BOOT_CMD sequential write: 0xFF, 0x00, 0x88, 0x55, 0xAA;
4. Enter the BOOT area instruction: BOOT_CMD sequential write: 0x37, 0xC8, 0x42, 0x9A, 0x65;

   Instructions response status:
   FLASH_BOOT_EN = 1: Indicates that it has entered Flash BOOT upgrade mode,
   FLASH_BOOT_EN = 0: Indicates that the Flash BOOT upgrade mode has been exited,
   ROM_OFFSETH/L address offset status:
   CFG_BOOT_SEL = 1, ROM_OFFSETH/L = 0x1000,
   If you are currently in the boot area:
   CFG_BOOT_SEL = 0, ROM_OFFSETH/L = 0x0000.
   Physical address of program execution = PC + ROM_OFFSETH/L.

Precautions;

1. When writing SPROG_CMD, BOOT_CMD instruction data, it must be written in order, otherwise it needs to be written again.
2. The working voltage of MCU is 2.7V~5.5V, and the MCU may work abnormally at 1.5V~2.7V, resulting in abnormal update and misoperation. Therefore, it is recommended not to perform IAP operation when the ADC or LVDT detection voltage is lower than 2.7 V before IAP operation .
3. It is recommended to shield the interrupt during the update process to ensure that the IAP operation will not be affected by the interruption, and resume the interruption after the IAP operation is completed, and perform data verification after updating the data to ensure that the data is updated correctly.

17.3.4. Address Correspondence in BOOT Upgrade Mode

Address correspondence in BOOT upgrade mode				
SPROG_ADDR_H[5:1]	Block	Byte write physical address corresponding range (HEX)		
8	8	00001000	--->	000011FF
9	9	00001200	--->	000013FF
10	10	00001400	--->	000015FF
11	11	00001600	--->	000017FF
12	12	00001800	--->	000019FF
13	13	00001A00	--->	00001BFF
14	14	00001C00	--->	00001DFF
15	15	00001E00	--->	00001FFF
16	16	00002000	--->	000021FF
17	17	00002200	--->	000023FF
18	18	00002400	--->	000025FF
19	19	00002600	--->	000027FF
20	20	00002800	--->	000029FF
21	21	00002A00	--->	00002BFF
22	22	00002C00	--->	00002DFF
23	23	00002E00	--->	00002FFF
24	24	00003000	--->	000031FF
25	25	00003200	--->	000033FF
26	26	00003400	--->	000035FF
27	27	00003600	--->	000037FF
28	28	00003800	--->	000039FF
29	29	00003A00	--->	00003BFF
30	30	00003C00	--->	00003DFF

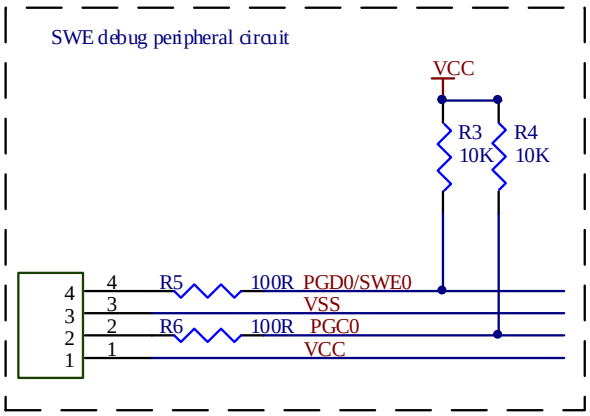
Note:

1. Byte write physical address corresponding register: {SPROG_ADDR_H[5:0], SPROG_ADDR_L[7:0]};
2. 512Bytes per Block;
3. When operating the 4K Block where the BOOT is located, the BOOT is write-protected and the operation is invalid;
4. When the BOOT function is used, all CODE areas of the program need to subtract the offset address of ROM_OFFSET_H/L (PC-ROM_OFFSET) to access the absolute address of the CODE area.

18. Burning and Debugging

18.1. SWE Circuit Connection

Two-wire programming and single-wire debugging. When performing simulation debugging, you need to connect a SWE wire. In the SWE debugging mode, the IO function of the SWE port is blocked. It is recommended not to configure other functions of the SWE debugging I/O port to avoid affecting the SWE debugging function.



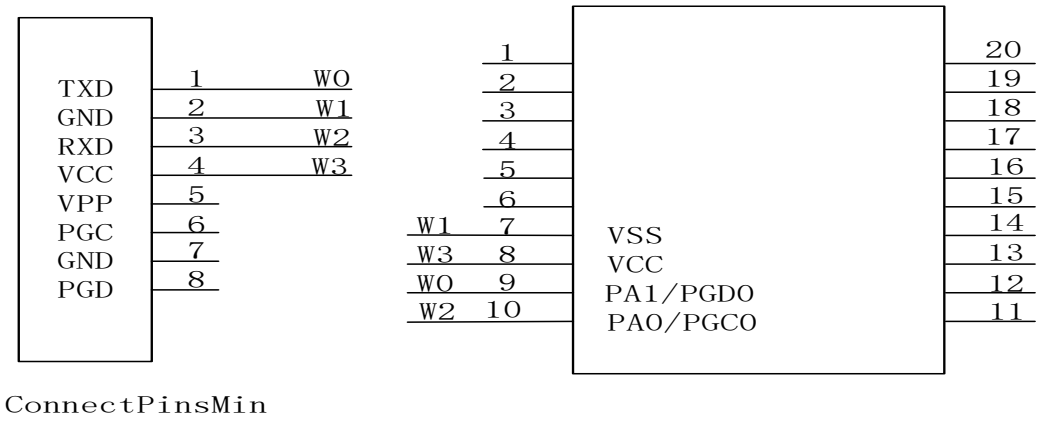
SWE circuit connection

18.2. TouchKey Programming

Connect the chip PGC0 (PGC1/PGC2), PGD0 (PGD1/PGD2), VCC, VSS four lines. When entering the programming interface, select the chip of the corresponding model. Open the compiled HEX file, click on a built-in flash to wait for burning.

When entering the debugging interface, first burn the HEX file with the debug data transmission mode, click to open the debug to view the touch key data.

For example:



BF7812AM20-TJLX burning wiring diagram

Notes: refer to the TK programming guide for specific operation instructions.

19. CPU Instruction System

19.1. Instruction Code

The BF7812AMXX-XJLX instructions are divided into signal-byte instructions, double-byte instructions and three-byte instructions.

Signal-byte instructions: A signal-byte instruction consists of 8 bit binary code. There are only instruction opcodes in the instruction, no instruction operand or instruction operand is implied in the instruction opcode. There are 49 such instructions.

Double-byte instructions: Consists of two bytes, one for opcode and the other for the operand (or operand address), stored in order in program memory. There are 46 such instructions.

Three-byte instructions: Consists of one byte of instruction opcode and two bytes of operands (or operand address). There are 16 such instructions.

19.2. Instruction Set

In order to describe the instructions conveniently, some symbols are used in the instructions. The meanings of these symbols are as follows:

addr 11	Lower 11 address
addr 16	16-bit address
direct	Direct addressing, 8-bit internal data and address (including special function registers)
bit	Bit address
#data	8-bit immediate
#data16	16-bit immediate
rel	Signed 8-bit relative displacement
n	Number 0~7
Rn	R0~R7 working registers of the current register group
i	Numbers 0, 1
Ri	Working register R0, R1
@	Register indirect addressing
←	Data transfer direction
∧	Logical "and"
∨	Logical OR
⊕	Logical "exclusive OR"
√	Affect the flag
×	No effect on the flag

CPU instruction symbol meaning table

Provides the assembly instructions used, the function of each instruction, the number of bytes occupied, the execution cycle of the instruction, and the effect on the corresponding flags:

8 bit data transfer instructiion								
Mnemonic		Function	Impact on the flag				Number of bytes	Number of cycles
			P	OV	AC	CY		
MOV A	Rn	A←(Rn)	√	×	×	×	1	1
	direct	A←(direct)	√	×	×	×	2	1
	@Ri	A←((Ri))	√	×	×	×	1	1
	#data	A←data	√	×	×	×	2	1
MOV Rn	A	Rn←(A)	×	×	×	×	1	1
	direct	Rn←(direct)	×	×	×	×	2	2
	#data	Rn←data	×	×	×	×	2	1
MOV direct1	A	direct1←(A)	×	×	×	×	2	1
	Rn	direct1←(Rn)	×	×	×	×	2	1
	direct2	direct1←(direct2)	×	×	×	×	3	2
MOV direct,	@Ri	direct←((Ri))	×	×	×	×	2	2
	#data	direct←data	×	×	×	×	3	1
MOV @Ri	A	(Ri)←(A)	×	×	×	×	1	1
	direct	(Ri)←(direct)	×	×	×	×	2	2
	#data	(Ri)←data	×	×	×	×	2	1
16 bit data transfer instruction								
Mnemonic		Function	Impact on the flag				Number of bytes	Number of cycles
			P	OV	AC	CY		
MOV DPTR,#data16		DPTR←data16	×	×	×	×	3	1
External data transfer and table lookup instructions								
Mnemonic		Function	Impact on the flag				Number of bytes	Number of cycles
			P	OV	AC	CY		
MOVX @DPTR,A		(DPTR)←(A)	×	×	×	×	1	1
MOVC A,	@A+DPTR	A←((A)+(DPTR))	√	×	×	×	1	1
	@A+PC	A←((A)+(PC))	√	×	×	×	1	1
MOVX A,	@DPTR	A←(DPTR)	√	×	×	×	1	1
Notes: The number of cycles and the number of bytes of the MOVX instruction can be configured through registers CKCON<2:0>.								
Exchange class instruction								
Mnemonic		Function	Impact on the flag				Number of bytes	Number of cycles
			P	OV	AC	CY		
XCH A,	Rn	(Rn)←(A)	√	×	×	×	1	1
	direct	(A)←(direct)	√	×	×	×	2	2

	@Ri	(A)←((Ri))	×	×	×	×	1	2
XCHD A,@Ri		(A)3~0~((Ri))3~0	√	×	×	×	1	2
SWAP A		(A)7-4~(A)3-0	√	×	×	×	1	1
Arithmetic operation instruction								
Mnemonic		Function	Impact on the flag				Number of bytes	Number of cycles
			P	OV	AC	CY		
ADD A	Rn	A←(A)+(Rn)	√	√	√	√	1	1
	direct	A←(A)+(direct)	√	√	√	√	2	2
	@Ri	A←(A)+((Ri))	√	√	√	√	1	2
	#data	A←(A)+data	√	√	√	√	2	1
ADDC A	Rn	A←(A)+(Rn)+(C)	√	√	√	√	1	1
	direct	A←(A)+(direct) +(C)	√	√	√	√	2	2
	@Ri	A←(A)+((Ri)) +(C)	√	√	√	√	1	2
	#data	A←(A)+data+(C)	√	√	√	√	2	1
INC	A	A←(A)+1	√	×	×	×	1	1
	Rn	Rn←(Rn)+1	×	×	×	×	1	1
	direct	direct←(direct)+1	×	×	×	×	2	2
	@Ri	(Ri)←((Ri))+1	×	×	×	×	1	2
	DPTR	DPTR←((DPTR))+1	×	×	×	×	1	1
DA A		BCD code adjustment	√	×	√	√	1	1
SUBB A	Rn	A←(A)-(Rn)-(C)	√	×	×	×	1	1
	direct	A←(A)-(direct)-(C)	√	√	√	√	2	2
	@Ri	(A)←(A)-((Ri))-(C)	√	√	√	√	1	2
	#data	A←(A)-data-(C)	√	√	√	√	2	1
DEC	A	A←(A)-1	√	×	×	×	1	1
	Rn	Rn←(Rn)-1	×	×	×	×	1	1
	direct	direct←(direct)-1	×	×	×	×	2	2
	@Ri	(Ri)←((Ri))-1	×	×	×	×	1	2
MUL AB		BA←(A)*(B), after performing the multiplication operation, the lower byte is stored in A and the high byte is stored in B.	√	√	×	0	1	1
DIV AB		A←(A)/(B) B←remainder	√	√	×	0	1	1
Notes: When the DA instruction is used, the adjustment rules are as follows: if the low 4 bits of accumulator A are greater than 9 or AC=1, then A←A+06H; if the high 4 bits of accumulator A								

are greater than 9 or CY=1, then A←A+60H.								
Logical operation instruction								
Mnemonic		Function	Impact on the flag				Number of bytes	Number of cycles
			P	OV	AC	CY		
CLR A		A←00H	√	×	×	×	1	1
CPL A		A←($\overline{A}$)	√	×	×	×	1	1
ANL A,	Rn	A←(A)∧(Rn)	√	×	×	×	1	1
	direct	A←(A)∧(direct)	√	×	×	×	2	2
	@Ri	A←(A)∧((Ri))	√	×	×	×	1	2
	#data	A←(A)∧data	√	×	×	×	2	1
ANL direct,	A	direct←(A)∧(direct)	×	×	×	×	2	2
	#data	direct←(direct)∧data	×	×	×	×	3	2
ORL A,	Rn	A←(A)∨(Rn)	√	×	×	×	1	1
	direct	A←(A)∨(direct)	√	×	×	×	2	2
	@Ri	A←(A)∨((Ri))	√	×	×	×	1	2
	#data	A←(A)∨data	√	×	×	×	2	1
ORL direct,	A	direct←(direct)∨(A)	×	×	×	×	2	2
	#data	direct←(direct)∨data	×	×	×	×	3	2
XRL A,	Rn	A←(A)⊕(Rn)	√	×	×	×	1	1
	direct	A←(A)⊕(direct)	√	×	×	×	2	2
	@Ri	A←(A)⊕((Ri))	√	×	×	×	1	2
	#data	A←(A)⊕data	√	×	×	×	2	1
XRL direct,	A	direct←(direct)⊕(A)	×	×	×	×	2	2
	#data	direct←(direct)⊕data	×	×	×	×	3	2
Loop, shift class instruction								
Mnemonic		Function	Impact on the flag				Number of bytes	Number of cycles
			P	OV	AC	CY		
RL A		The content in A is rotated left by one bit.	×	×	×	×	1	1
RLC A		A content with carry left shift one bit.	√	×	×	√	1	1
RR A		The content in A is rotated right by one bit.	×	×	×	×	1	1
RRC A		A content with carry right shift one bit.	√	×	×	√	1	1
Call, return class instruction								
Mnemonic		Function	Impact on the flag				Number of bytes	Number of cycles
			P	OV	AC	CY		

LCALL addr16	(PC)←(PC)+3,(SP)←(PC), (PC)←addr16	×	×	×	×	3	2
ACALL addr11	(PC)←(PC)+2,(SP)←(PC), (PC10~0)←addr11	×	×	×	×	2	2
RET	(PC)←((SP))	×	×	×	×	1	2
RETI	(PC)←((SP)) return from interrupt	×	×	×	×	1	2

Transfer class instruction

Mnemonic	Function	Impact on the flag				Number of bytes	Number of cycles
		P	OV	AC	CY		
LJMP addr16	PC←addr15~0	×	×	×	×	3	1
AJMP addr11	PC10~0←addr10~0	×	×	×	×	2	1
SJMP rel	PC←(PC)+rel	×	×	×	×	2	1
JMP @A+DPTR	PC←(A)+(DPTR)	×	×	×	×	1	1
JZ rel	PC←(PC)+2,If (A)=0, PC←(PC)+rel	×	×	×	×	2	2
JNZ rel	PC←(PC)+2, If (A)≠0, PC←(PC)+rel	×	×	×	×	2	2
JC rel	PC←(PC)+2, If (CY)=1, PC←(PC)+rel	×	×	×	×	2	2
JNC rel	PC←(PC)+2, If (CY)=0, PC←(PC)+rel	×	×	×	×	2	2
JB bit,rel	PC←(PC)+3, If (bit)=1, PC←(PC)+rel	×	×	×	×	3	2
JNB bit,rel	PC←(PC)+3, If (bit)=0, PC←(PC)+rel	×	×	×	×	3	2
JBC bit, rel	PC←(PC)+3, If (bit)=1,bit←0, PC←(PC)+rel	×	×	×	×	3	2

CJNE A, direct, rel	PC←(PC)+3,
	If (A) ≠direct,
	PC(PC)+rel
	If (A)<(direct),
		×	×	×	×	3	2

		CY←1						

	A,#data,rel	PC←(PC)+3,
		If (A) ≠data,
		PC(PC)+rel
		If (A)<(data), CY←1
			×	×	×	×	3	2

	Rn,#data,rel	PC←(PC)+3,
		If (Rn) ≠data,
		PC←(PC)+rel
		If (Rn)<(data), CY←1
			×	×	×	×	3	1

	@Ri,#data,rel	PC←(PC)+3, if ((Ri)) ≠data, PC←(PC)+rel If ((Ri))<(data), CY←1	×	×	×	×	3	2
DJNZ	Rn,rel	PC←(PC)+2,Rn←(Rn)-1, If (Rn) ≠0, PC←(PC)+rel	×	×	×	×	2	1
	direct,rel	PC←(PC)+3, (direct)←(direct)-1, if (direct) ≠0, PC←(PC)+rel	×	×	×	×	3	2

Stack, empty operation class instruction

Mnemonic	Function	Impact on the flag				Number of bytes	Number of cycles
		P	OV	AC	CY		
PUSH direct	SP←(SP)+1, (SP)←(direct)	×	×	×	×	2	2
POP direct	direct←(SP), SP←(SP)-1	×	×	×	×	2	2
NOP	empty operation	×	×	×	×	1	1

Bit manipulation instruction

Mnemonic		Function	Impact on the flag				Number of bytes	Number of cycles
			P	OV	AC	CY		
MOV	C, bit	CY←bit	×	×	×	√	2	2
	bit, C	bit←CY	×	×	×	×	2	2
CLR	C	CY←0	×	×	×	√	1	1
	bit	bit←0	×	×	×	×	2	2
SETB	C	CY←1	×	×	×	√	1	1
	bit	bit←1	×	×	×	×	2	2
CPL	C	CY←($\overline{CY}$)	×	×	×	√	1	1
	bit	bit←($\overline{bit}$)	×	×	×	×	2	2

ANL	C, bit	C←(C)∧(bit)	×	×	×	√	2	2
	C, /bit	C←(C)∧($\overline{bit}$)	×	×	×	√	2	2
ORL	C, bit	C←(C)∨(bit)	×	×	×	√	2	2
	C, /bit	C←(C)∨($\overline{bit}$)	×	×	×	√	2	2

Pseudo-instruction		
Mnemonic	Instruction format	Function description
ORG	【tab:】ORG addr16	Define the first address of tab
EQU	tab EQU data/tab	Assign values to labels
DB	【tab:】 DB item or item tabel	Define a-byte or multi-byte
DW	【tab:】 DW item or item tabel	16 bit word content used to define two or more cells in memory
DS	【tab:】DS expression	Specifies to leave several memory cells starting with the label
BIT	tab BIT address	Assign a bit address to a label
END	END is placed at the end of the assembly language program to tell the assembler that the source program ends here.	

CPU instruction set table

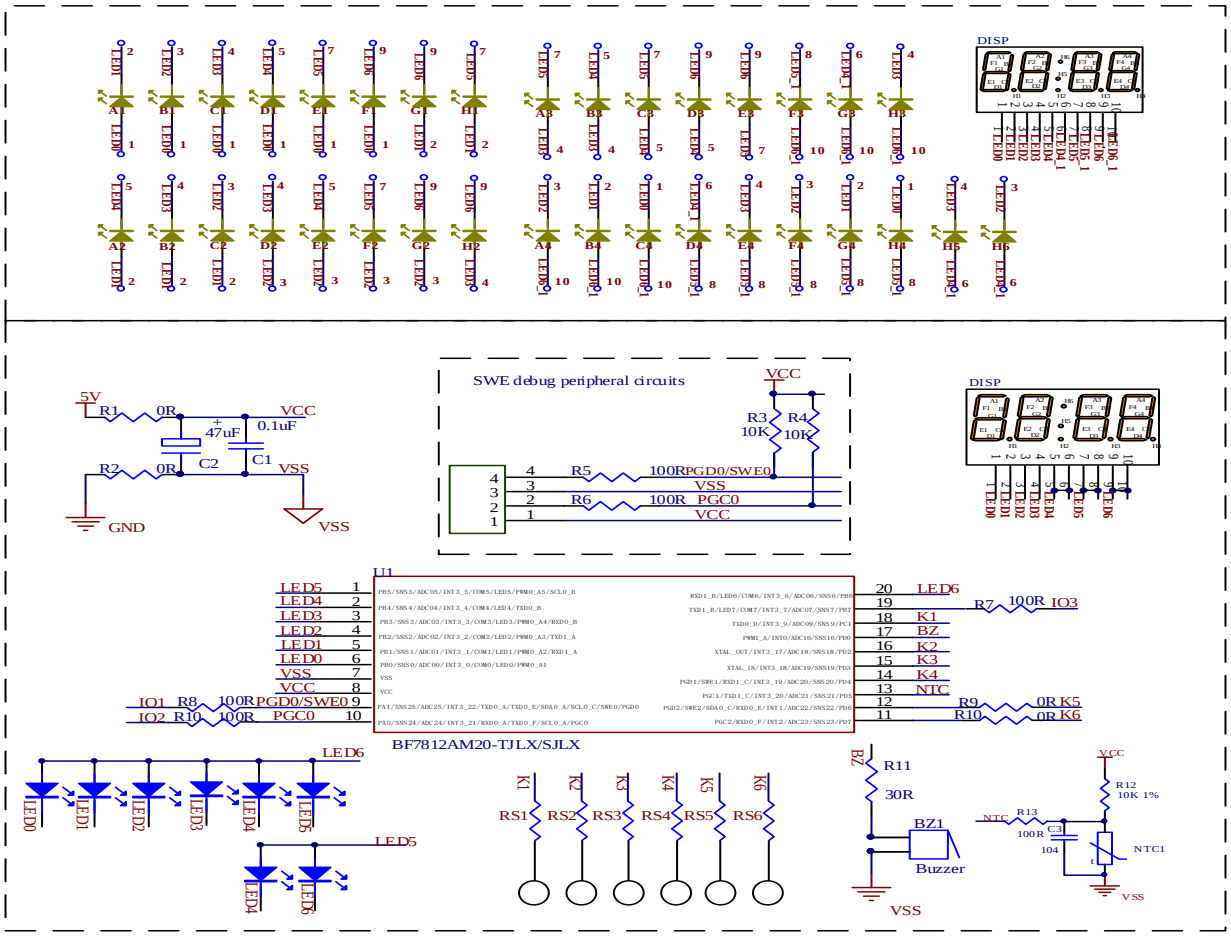
CPU related register

SFR register				
Address	**Name**	**RW**	**Reset value**	**Function description**
0x81	SP	RW	0x07	stack pointer register
0x82	DPL	RW	0x00	data pointer register 0 low 8 bit
0x83	DPH	RW	0x00	data pointer register 0 high 8 bit
0x87	PCON	RW	0x00	idle mode 1 select register
0xE0	ACC	RW	0x00	accumulator
0xF0	B	RW	0x00	B register

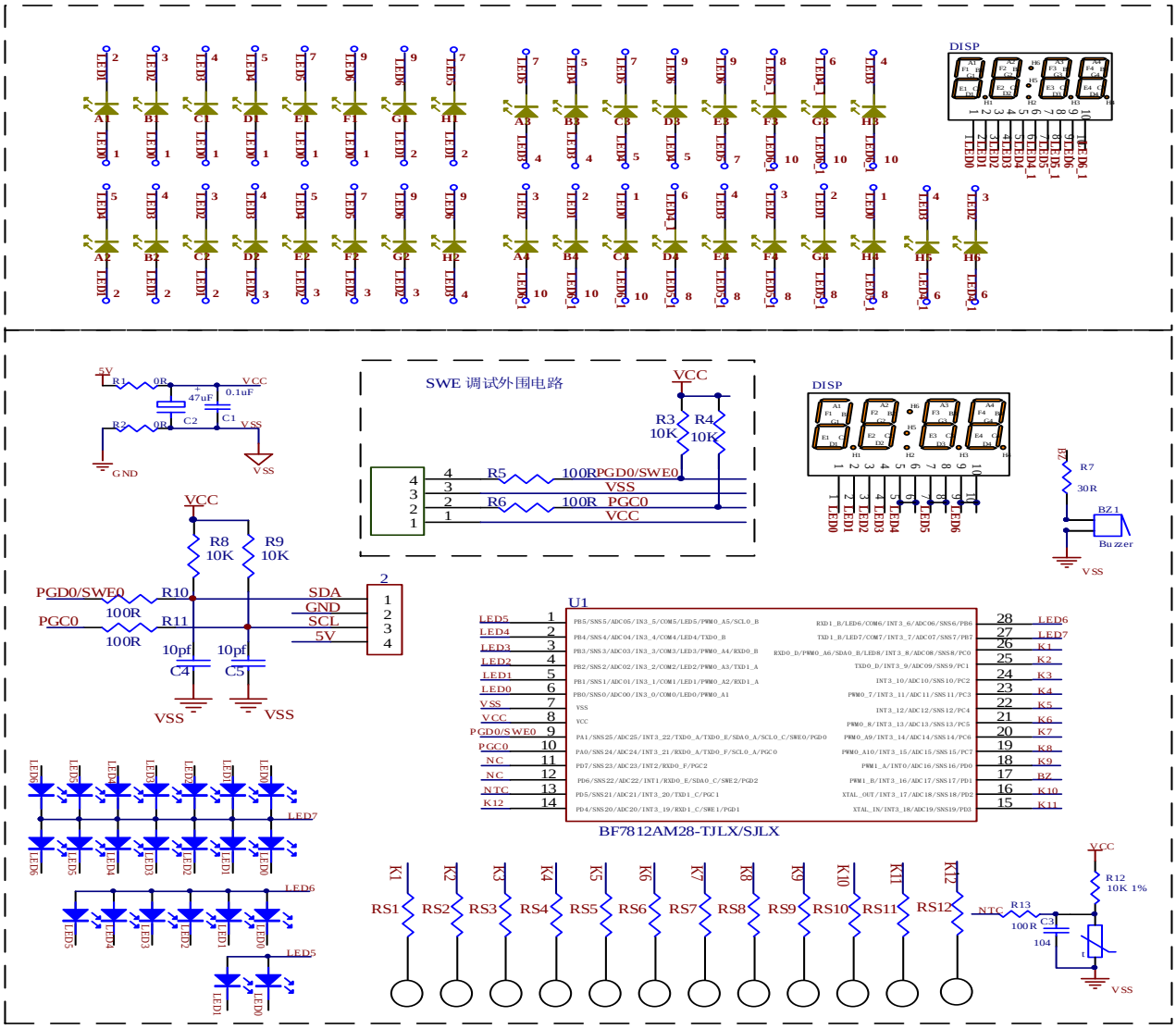
CPU SFR register list

20. Reference Application Circuits

20.1. BF7812AM20-TJLX/SJLX Reference Circuit



20.2. BF7812AM28-TJLX/SJLX Reference Circuit

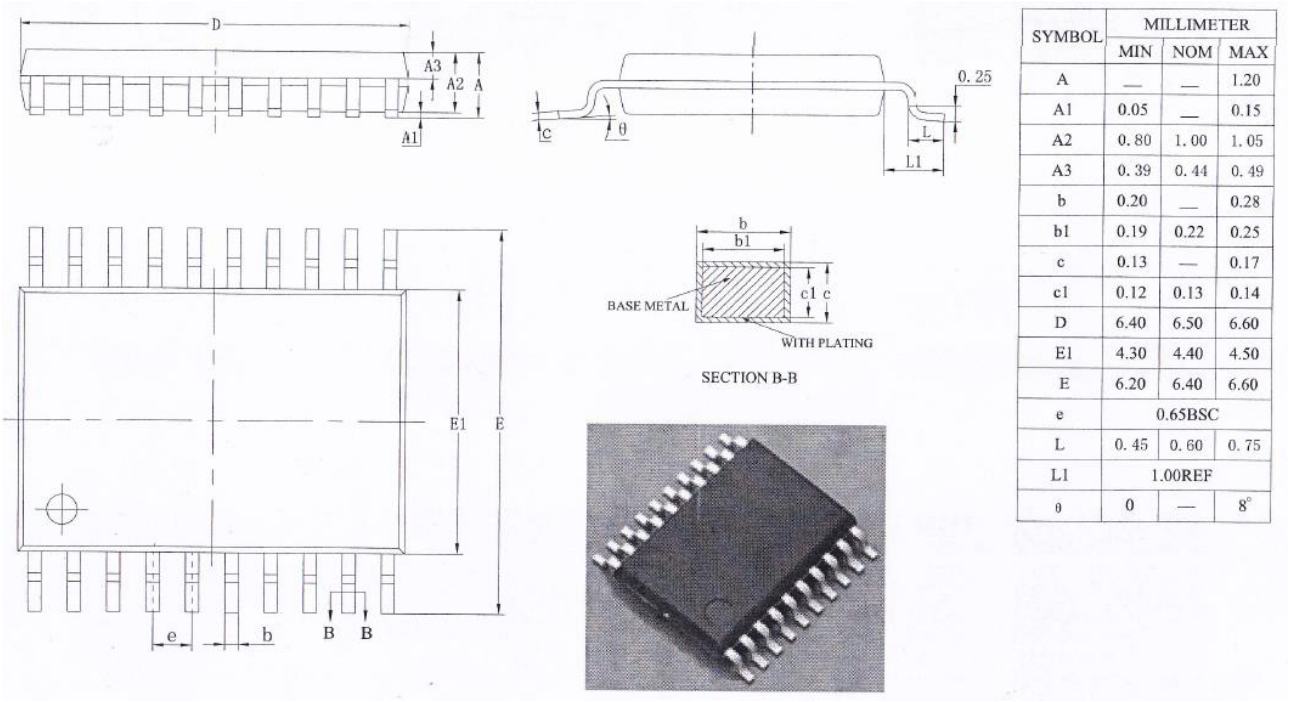


Note:

1. The above reference schematic reference circuit is for reference design only.
2. The RSX channel resistance is recommended to be 1k~8.2k, normal 4.7k.
3. The SWE debugging peripheral circuit is only used for SWE debugging. If the emulator or adapter board has a pull-up resistor, there is no need to connect the SWE pull-up resistor.
4. Replace the 0Ω resistors with parallel power and ground with magnetic beads. The EMI test item (RE) can increase the test margin. The recommended parameter is 600 Ω@100MHz.

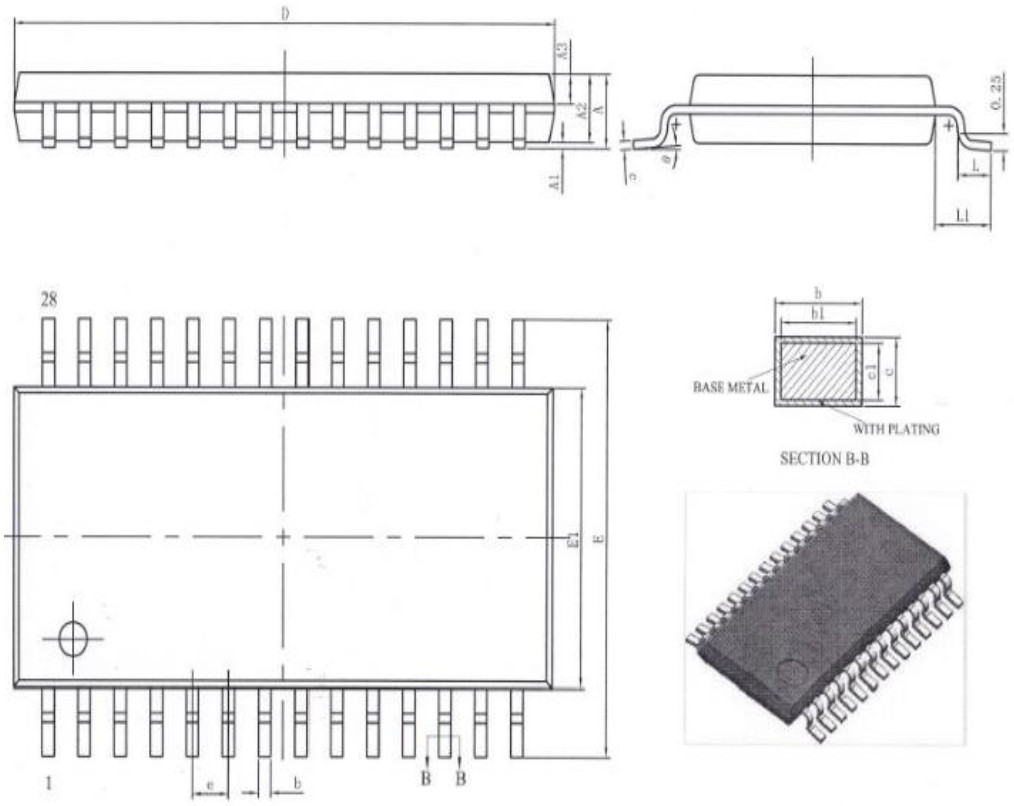
21. Packages

21.1. TSSOP20



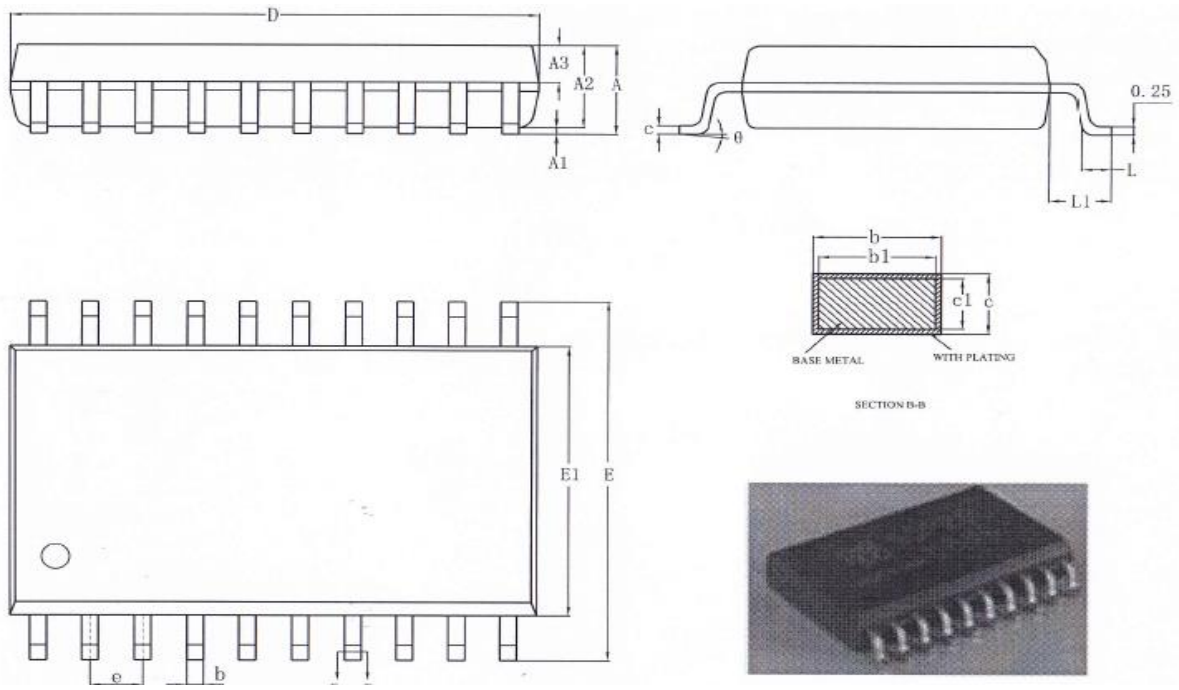
SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.20
A1	0.05	—	0.15
A2	0. 80	1. 00	1. 05
A3	0. 39	0. 44	0. 49
b	0.20	—	0.28
b1	0.19	0.22	0.25
c	0.13	—	0.17
c1	0.12	0.13	0.14
D	6.40	6.50	6.60
E1	4.30	4.40	4.50
E	6.20	6.40	6.60
e	0.65BSC		
L	0. 45	0. 60	0. 75
L1	1.00REF		
θ	0	—	8°

21.2. TSSOP28



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.20
A1	0.05	—	0.15
A2	0.80	—	1.00
A3	0.39	0.44	0.49
b	0.20	—	0.29
b1	0.19	0.22	0.25
c	0.14	—	0.18
c1	0.12	0.13	0.14
D	9.60	9.70	9.80
E	6.20	6.40	6.60
E1	4.30	4.40	4.50
e	0.65BSC		
L	0.45	0.60	0.75
L1	1.00BSC		
θ	0	—	8°

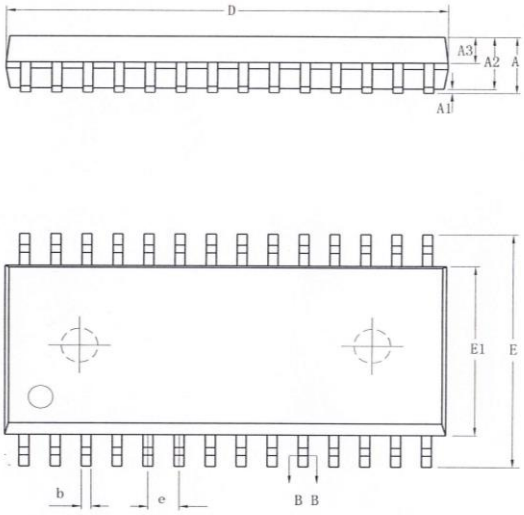
21.3. SOP20



DIM	SOP20 MILLIMETERS		
	MIN	NOM	MAX
A	-	-	2.650
A1	0.100	0.200	0.300
A2	2.250	2.300	2.350
b	0.350	-	0.440
c	0.250	-	0.310
D	12.600	12.800	13.000
E1	7.300	7.500	7.700
E	10.100	10.300	10.500
e	1.270(BSC)		
L	0.7	-	1
θ	0 °	-	8 °
end face waste glue	-	-	0.200
Overall length of plastic body	12.800	13.000	13.300

SOP20 package infographic

21.4. SOP28

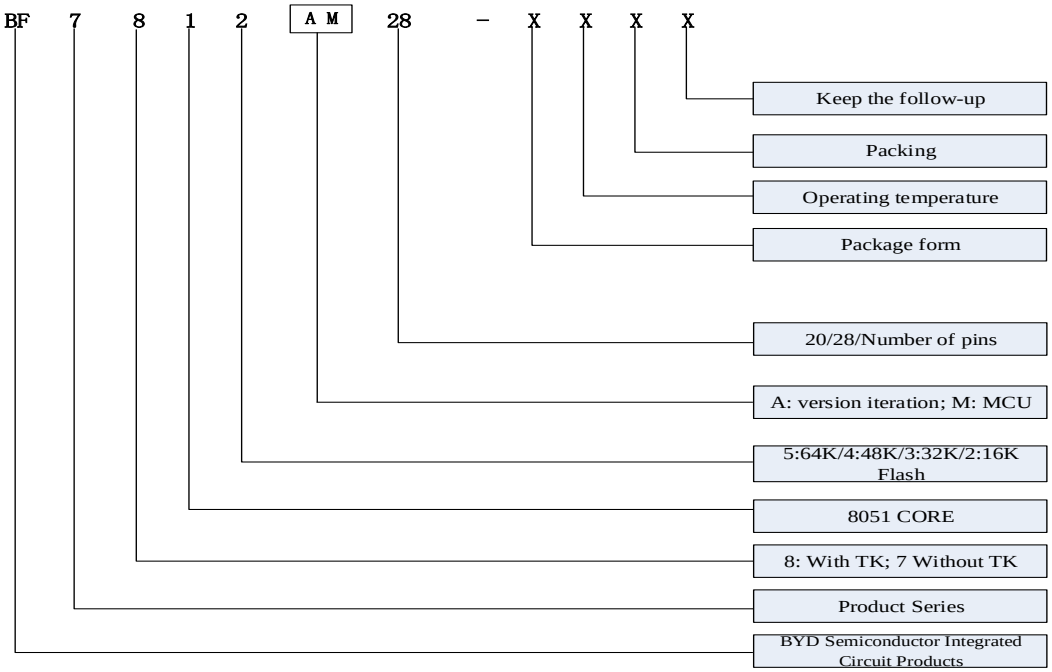


SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	2.65
A1	0.10	—	0.30
A2	2.25	2.30	2.35
A3	0.97	1.02	1.07
b	0.39	—	0.48
b1	0.38	0.41	0.43
c	0.25	—	0.31
c1	0.24	0.25	0.26
D	17.80	18.00	18.20
E	10.10	10.30	10.50
E1	7.30	7.50	7.70
e	1.27BSC		
L	0.70	—	1.00
L1	1.40BSC		
θ	0	—	8°

Ordering information

Package	Work temperature		Package style	Keep the follow-up
S: SOP	Car grade	A: -40℃~+150℃	B: tap	-
A: SSOP		B: -40℃~+125℃	L: feed tube	-
T: TSSOP		C: -40℃~+105℃	T: tray	-
M: MSSOP		D: -40℃~+85℃	-	-
L: LQFP	Industrial grade	K: -40℃~+85℃	-	-
Q: QFN		J: -40℃~+105℃	-	-
B: BGA		L: -40℃~+125℃	-	-
D: DIP	Consumer grade	P: -25℃~+70℃	-	-
-		Q: 0℃~+70℃	-	-

Example:



Revision History

Revised date	Revised content	Reviser	Remarks
2021-07-21	V1.0	YNN	V1.0
2021-08-25	1. Update the BFH, A2H, AAH, B5H, BBH, C7H registers 2. Delete CTK parallel mode 3. Add BOR description 4. Update the reset sequence 5. Update Reference Circuit	YNN	V1.1
2021-11-03	1. Update the brown-out reset voltage range 2. Update the LVDT detection voltage range 3. Timer 0/1 delete counting function 4. Update the 89H, C4H, FFH register	YNN	V1.2
2022-03-09	1. Update storage description 2. "EEPROM " name updated to "DATA area" 3. Update header 4. Update clock block diagram 5. Update instruction set	YNN	V1.3
2022-08-12	1. Added models: BF7812AM20-SJLX and BF7812AM28-SJLX 2. Updated description of ADC conversion time 3. Add the description of LED serial dot matrix scan time	YNN	V1.4
2022-10-10	1. Delete the SSOP28 package model	YNN	V1.5

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